SiliconGraphics
Computer Systems

Indigo²™
Technical Report

IRIS Indigo^2 Technical Report

Version 2.0

Copyright 1993 Silicon Graphics, Inc. All rights reserved.

This document was contains proprietary and confidential information of Silicon Graphics, Inc. The contents of this document may not be disclosed to third parties, copied or duplicated in any form, without the prior written permission of Silicon Graphics, Inc. The receipt or possession of this document does not convey any right, title, or interest, either directly or by implication, estoppel, or otherwise, under any trade secret, copyright, trademark, patent, patent application or other intellectual property right.

IRIS, Silicon Graphics, the Silicon Graphics logo, and Geometry Engine are registered trademarks and Indigo, IRIS Indigo, Indigo^2, Elan Graphics, Galileo Video, IRIS 4D, Virtual24, IRIX, 4DWM, Graphics Library, IRIS GL, Open GL, GE7, IRIS POWERVision, IRIS WorkSpace, IRIS InSight, CaseVision, ImageVision Library, NetVisualyzer, 4DDN, IRIS Explorer, and IRIS Showcase are trademarks of Silicon Graphics, Inc.

Apple and Macintosh are registered trademarks of Apple Computer, Inc. IBM, PS/2, and RS/6000 are registered trademarks of International Business Machines, Inc. Intel and i860 are registered trademarks of the Intel Corporation. DECnet is a trademark of Digital Equipment Corporation. Ethernet is a registered trademark of Xerox Corporation. R3000A, R4000SC, and R4400SC are trademarks of MIPS Technology, Inc. Motif is a registered trademark of Open Software Foundation. UNIX is a registered trademark of Unix Systems Laboratories. X-Window System is a trademark of the Massachusetts Institute of Technology. NFS is a trademark of Sun Microsystems, Inc.

U.S. Government Users: If this document is acquired by or on behalf of an entity of the United States Government, the following provision applies:

U.S. GOVERNMENT LIMITED RIGHTS LEGEND

Use, duplication or disclosure by the Government of the limited rights data set forth herein is subject to restrictions as set forth in FAR 52.227-14(g)(2) or subparagraph (b)(3) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013 and/or in similar or successor clauses in the FAR, or the DOD or NASA FAR Supplement. Such restrictions are not subject to an expiration date. Unpublished-rights reserved under the Copyright Laws of the United States. Contractor/manufacturer is SILICON GRAPHICS INC., 2011 N. Shoreline Blvd.,Mountain View, CA 94039-7311.

Published in the United States of America. The specifications noted in this document are subject to change without notice.

Table of Contents

1 IRIS Indigo2 Overview 5
- 1.1 Indigo2 CPUs 6
- 1.2 Indigo2 Graphics 6
- 1.3 Indigo2 Technology 6
- 1.4 Indigo2 Audio and Video 7
  - 1.4.1 Galileo Video™ 7

2 The IRIS Indigo2 Workstation 8
- 2.1 Standard Equipment 8
  - 2.1.1 Drive Bays 9
  - 2.1.2 Ports 9
- 2.2 Optional Peripherals 9
  - 2.2.1 3.5" Internal Devices 9
  - 2.2.2 5.25" Internal Devices 10
  - 2.2.3 External Devices 10

3 IRIS Indigo2 CPU Boards 12
- 3.1 Processor Core 14
- 3.2 GIO64 Bus 18
- 3.3 EISA Bus 18
- 3.4 Main Memory 19
- 3.5 The I/O System 20
- 3.6 The Audio System 21
  - 3.6.1 HAL2 ASIC 22
  - 3.6.2 Codecs 23
  - 3.6.3 Serial Digital Audio Transmitter 23
  - 3.6.4 Serial Digital Audio Receiver 24
  - 3.6.5 Microphone 24
  - 3.6.6 Internal Speaker 24
  - 3.6.7 Headphone Output 24
- 3.7 Expansion Slots 24

4 XL Graphics 25
- 4.1 Graphics Processing 26
- 4.2 The Raster Engine 28
- 4.3 Framebuffer and Clipping Planes 29
- 4.4 Color Lookup 30

5 XZ and Extreme Graphics 31
- 5.1 Features 31
- 5.2 VLSI Integration 32
- 5.3 Graphics Architecture 33
- 5.4 The CPU Interface 33
- 5.5 Packaging 34
- 5.6 Graphics Hardware 34
  - 5.6.1 Command Engine 34
  - 5.6.2 Geometry Subsystem 38
  - 5.6.3 Raster Subsystem 40
  - 5.6.4 Display Subsystem 43

5.7 XZ and Extreme Graphics Features 44
5.7.1 MicroPixel Sub-Pixel Positioning 44
5.7.2 Blending 44
5.7.3 Point Anti-Aliasing 45
5.7.4 Line Anti-Aliasing 45
5.7.5 SharpScene Accumulation Buffer 45
5.7.6 Lighting Features 46
5.7.7 Atmospheric Effects 47
5.7.8 Texture Mapping 47
5.7.9 Stencil Planes 48
5.7.10 Arbitrary Clipping Planes 48
5.7.11 Pixel Read, Write, and Copy 49

6 Software Environment 50
6.1 End User Tools 50
6.1.1 IRIS InSight™ Viewer 50
6.1.2 Space Tour 50
6.1.3 WorkSpace 51
6.1.4 System Manager 51
6.1.5 IRIS Showcase™3.0 51
6.1.6 IRIS Media Mosaic 51
6.1.7 ImageTools 51
6.1.8 Digital Media Clip Library 52
6.1.9 IRIS Explorer 52
6.2 Developer Tools 52
6.2.1 CASEVision 53
6.2.2 Compilers and Standard Development Tools 53
6.2.3 The Iris Graphics Library 53
6.2.4 Open GL 54
6.2.5 IRIS Inventor 54
6.2.6 Image Processing Library 55
6.2.7 Digital Media Libraries 55
6.3 Operating System 55
6.3.1 IRIX 5.1 55
6.3.2 The X Window System 56
6.4 Networking 57

Section 1 IRIS Indigo^2 Overview

As a member of the IRIS 4D™ family of graphics workstations, Indigo^2™ offers the powerful, interactive 3D graphics that have made Silicon Graphics the industry leader in technical, scientific, and creative computing. As a full-featured UNIX® workstation, Indigo^2 offers network file access, virtual memory, multitasking, and all the UNIX standards that technical users demand. As a next-generation workstation, Indigo^2 adds features such as DAT-quality audio processing, a modular design allowing an easy upgrade of CPU board, graphics board, or memory configuration, and an option for live video I/O that make it ideal for professional multimedia authoring.

Figure 1 illustrates the Indigo^2 central unit with an attached monitor, keyboard, three button mouse, and microphone.The Indigo^2 central unit measures 5.0 inches high by 18.5 inches wide by 18.5 inches deep. Its shape and sturdy construction allow it to be placed beneath a 19" monitor or stand upright on its side.

FIGURE 1 Indigo^2 with accompanying keyboard, mouse, monitor, and microphone.

The Indigo^2 central unit houses a power supply, a speaker, a hard disk drive, and slots for additional data storage devices such as CD–ROM, DAT, and floppy disk drives. A door on the front of the unit provides easy access to removable media. All internal drives are front loading and self-configuring; they can be effortlessly removed and re-installed at sites that require security. The top of the unit can be lifted off to access memory, CPU daughter card, power supply, printed circuit boards, and expansion slots.

Indigo^2 has four expansion slots; all four slots have EISA bus connectors, two of the slots have GIO64 pipelined bus connectors as well. The EISA bus fully conforms to version 3.12 of the EISA standard allowing the use of a large variety of EISA and ISA expansion cards.

1.1 Indigo^2 CPUs

The Indigo^2 workstation comes in two, easy-to-upgrade CPU module configurations:

- R4000SC version, based on the MIPS R4000SC CPU
- the faster, more powerful R4400SC version, based on the MIPS R4400SC CPU

Indigo^2 offers a new generation of system architecture designed to take full advantage of the these CPUs. The Indigo^2 system buses and main memory buses have been increased to 64 bits to take advantage of the 64–bit wide processor bus of the R4000SC and R4400SC CPUs. The 64-bit wide system bus in Indigo^2 runs at 400 MB per second and can transfer data at 266 MB per second. Primary data and instruction caches of 8 KB each (16 KB each in the R4400SC version) combined with 1 MB of secondary cache and two Fast SCSI-2 channels add to the astonishing performance of the newest member of the Indigo family.

1.2 Indigo^2 Graphics

Indigo^2 can be configured with XL Graphics, XZ Graphics, or Extreme Graphics. XL Graphics is the Indigo^2 entry graphics subsystem. It makes extensive use of the power of the R4000/R4400 CPU by implementing the IRIS Graphics Library™ application programming interface as a set of highly efficient software algorithms.

XZ Graphics provides two Geometry Engine processors, a raster engine, high resolution full 24-bit color, and a built-in 24-bit Z-buffer. Extreme Graphics provides eight Geometry Engine processors, two raster engines, high resolution 24-bit color, and a 24-bit Z-buffer. Extreme Graphics is the most powerful graphics hardware currently offered by Silicon Graphics for a desktop workstation.

1.3 Indigo^2 Technology

To accelerate data transfer between the CPU and the graphics and I/O subsystems, Indigo^2 workstations use custom ASICs (Application-Specific Integrated Circuits) designed by Silicon Graphics. These chips manage memory and processor interrupts, handle I/O, control the bus, fill pixels and draw lines, control graphics output, and access color tables, often without CPU intervention. The result is a sustained data-transfer rate of up to 266 MB/second for the R4000SC and R4400SC 's direct CPU-to-RAM transfers.

To take advantage of improving technology, Indigo^2 clocks the CPU and system buses independently. This not only allows both the system bus and the CPU to run at maximum performance, it also allows upgrades to the CPU and graphics to occur independently.

To help speed the transfer of large blocks of data such as frames of bitmapped images used in animation, Indigo^2 workstations include a custom chip that supports Virtual DMA (Direct Memory Access). The chip knows the exact physical memory address of each page of virtual memory. A user can request DMA access to a data block using virtual memory addresses; the DMA engine provides direct access to the physical memory where the data is stored, even if the block is stored in discontinuous memory. Virtual DMA reduces interrupts and CPU overhead, and runs at maximum speed no matter how busy the operating system is.

Indigo^2 supports Fast SCSI-2 for maximum data transfer speed to SCSI devices via a SCSI-2 bus. The SCSI-2 bus operates at up to 10 MB per second on both SCSI-2 channels simultaneously. This bus can support internal hard drives of over one gigabyte of formatted capacity.

1.4 Indigo^2 Audio and Video

Indigo^2 workstations offer sound accompaniment to their graphic images with an audio system that supports 24-bit digital stereo and 16-bit analog stereo sound. It includes line-level and mic-level analog inputs, line-level analog outputs and, for working directly with digital audio, a stereo serial digital input/output jack.

Because many users want to mix incoming video with graphics and to record their work on videotape, Indigo^2 graphics boards include a bus to accept an add-on Silicon Graphics video board that handles composite or SVideo signals in NTSC or PAL formats.

1.4.1 Galileo Video™

Galileo Video is a video option from Silicon Graphics that transforms an Indigo^2 into a professional grade video production console. Some of the many features of Galileo Video include:

- NTSC and PAL standards
- professional quality Y/R-Y/B-Y and RGB formats
- industrial quality S-video and composite formats
- real-time and frame-by-frame video output and video-in-a-window display
- capture of video clips and frames to RAM or disk
- real-time video capture with the Cosmo™ Compression option
- Genlock to video input or external blackburst
- output of video sync
- SMPTE Vertical Interval Time Code support
- 8-bit per component 4:2:2 YUV color space with no conversions

Real-time processing is designed into the Galileo Video architecture. The alpha blending and key generator features enable on-line editing of many fundamental video effects:

- overlays
- dissolves
- fades
- wipes
- chroma keying
- luma keying

Section 2 The IRIS Indigo^2 Workstation

The Indigo^2 workstation was designed to be easy to set up, easy to use, easy to maintain, and easy to upgrade. The shape of the Indigo^2 allows it to be placed under a large monitor to save desk space or be placed vertically on its side. The various components that make up the Indigo^2 system have all been designed to get the user up and running quickly and yet provide the flexibility so important in a high-end workstation:

- Boards and internal devices are easy to access. Boards are accessible by removing the Indigo^2 top panel; internal devices are accessible by opening a front panel.
- Internal SCSI devices are self-configuring, and slide into and out of their slots in seconds.
- New input devices include a new PS/2®–standard keyboard and PS/2–standard mouse, or you can attach any other compatible PS/2–standard keyboard and mouse.
- An internal speaker is included for sound output, and a microphone provided for sound input.
- Expansion slots provide both GIO64 and EISA connectors.
- Iconic labels on all input and output connections, provide an intuitive, international recognition.

2.1 Standard Equipment

The following equipment is included as standard equipment with Indigo^2:

Display

- 19" Monitor (standard with XZ and Extreme Graphics)
  - 19" dual scan RGB monitor
  - 1280 x 1024 resolution
  - 60/72 Hz refresh rate
- 16" Monitor (standard with XL Graphics)
  - 16" dual scan RGB monitor
  - 1280 x 1024 resolution
  - 76 Hz refresh rate

Keyboard

- New full-size PS/2–standard keyboard with 15 function keys, numeric keypad, arrow keys, page-up, page-down, etc.

Mouse

- New PS/2–standard 3-button mechanical mouse

Microphone .

- Omnidirectional electret condenser microphone powered by system
- Frequency response: +/- 2 dB, 40 Hz to 18 kHZ
- 10' cord
- Lavalier microphone clip

Speaker

- 1.5 W internal (monural)
- Frequency response: 200 Hz -12 kHz

2.1.1 Drive Bays

Indigo^2 has one 5.25" half-height drive bay and two 3.5" drive bays.

2.1.2 Ports

On the back of the central unit are a number of industry-standard ports which can be used to connect other devices:

- A PS/2–standard keyboard port
- A PS/2–standard mouse port
- A high-density Fast SCSI-2 port for external SCSI devices such as disk drives and CD-ROMs
- An Ethernet port supporting both AUI and a 10Base-T (auto selecting) for connecting to local networks
- A bi-directional Centronics parallel port for color printers, scanners, and other parallel devices
- Two serial ports for modems, laser printers, MIDI devices, and other serial devices
- A stereo line-in jack for analog audio input from a tape deck, CD player, or similar source
- A stereo line-out jack for analog audio output to a tape deck, amplifier, or similar destination
- A microphone input jack for a mic-level audio input
- A headphone stereo output jack
- A digital input/output jack for serial digital audio input and output

2.2 Optional Peripherals

Indigo^2 has optional external peripherals as well as internal devices in both the 5.25" and 3.5" formats.

2.2.1 3.5" Internal Devices

Hard Drives

- Available in 236 MB, 535 MB, or 1.0 GB formatted capacity
- 10 MB burst-mode transfer rate for Fast SCSI-2
- SCSI-2 interface

Floppy Drive

- 1.44 MB formatted capacity
- UNIX compatible (using tar or cpio)
- PC compatible

DAT Drive

- 1.3 or 2.0 Gb capacity
- 4mm DAT metal particle tape
- 3.5" half-height form factor
- SCSI-2 interface
- 183 kByte/sec sustained transfer rate
- 5 MB/sec burst transfer rate
- <20 sec average access time
- DAT-quality audio over SCSI bus

2.2.2 5.25" Internal Devices

Hard Drives

- an adapter is available that fits the 1.0 Gb internal 3.5" hard disk into the 5.25" drive bay. The hard disk maintains the same formatted capacity, SCSI-2 interface and transfer rates.

CD-ROM Drive

- Dual speed
- 600 MB capacity (12 cm disc)
- 300 kB/sec sustained transfer rate
- SCSI-2 interface
- CD quality audio over SCSI bus

Tape Drive

- 1.0 GB 1/4" SCSI QIC tape drive

2.2.3 External Devices

Storage Devices

- 1.0 GB 1/4" SCSI QIC tape drive

CD-ROM Drive

- Dual speed
- 600 MB capacity (12 cm disc)
- 300 kB/sec sustained transfer rate
- SCSI-2 interface
- CD quality audio over SCSI bus

Input Devices

- Dials box
- Dials and buttons box
- Digitizer tablet with stylus (115V)
- Digitizer tablet cursor

Section 3 IRIS Indigo^2 CPU Boards

Indigo^2 is available with either the R4000SC or R4400SC CPU boards. The Indigo^2 version of these CPU boards offers several new features and enhancements:

- Indigo^2 uses pipelined GIO64 bus slots instead of GIO32 bus slots.
- The Indigo^2 I/O system includes two channels of Fast SCSI-2, 10Base-T Ethernet, and PS/2 standard keyboard and mouse ports.
- The Indigo^2 audio system offers a new enhanced audio system architecture.
- Indigo^2 includes four EISA bus connectors.

The Indigo^2 provides an easy upgrade path for newer and faster CPUs; the CPU and the second-level cache on the R4000SC/R4400SC board is mounted on an easily changed CPU module which can be swapped without changing the rest of the CPU board.

The R4000SC CPU module is based on the R4000SC CPU, which runs at 50 MHz externally and 100 MHz internally and includes data and instruction caches (8 KB each) and a high-performance FPU.

The R4400SC CPU module, based on the MIPS R4400SC CPU, is very similar in architecture to the R4000SC CPU module; however, the R4400SC CPU module is significantly faster. It runs at 75 MHz externally and 150 MHz internally and includes data and instruction caches of 16 KB each. Both the R4000SC and R4400SC includes a cache controller connected to an external second-level cache of 1 MB.

The R4000SC/R4400SC board's main memory capacity is a full 384 MB of DRAM. Because the board replaces SIMM-mounted DRAM interleave controllers with motherboard mounted DMUX chips, main memory is implemented with standard 36-bit-wide DRAM SIMMs.

The block diagram illustrated in Figure 2 illustrates the Indigo^2 R4000SC/R4400SC CPU board.

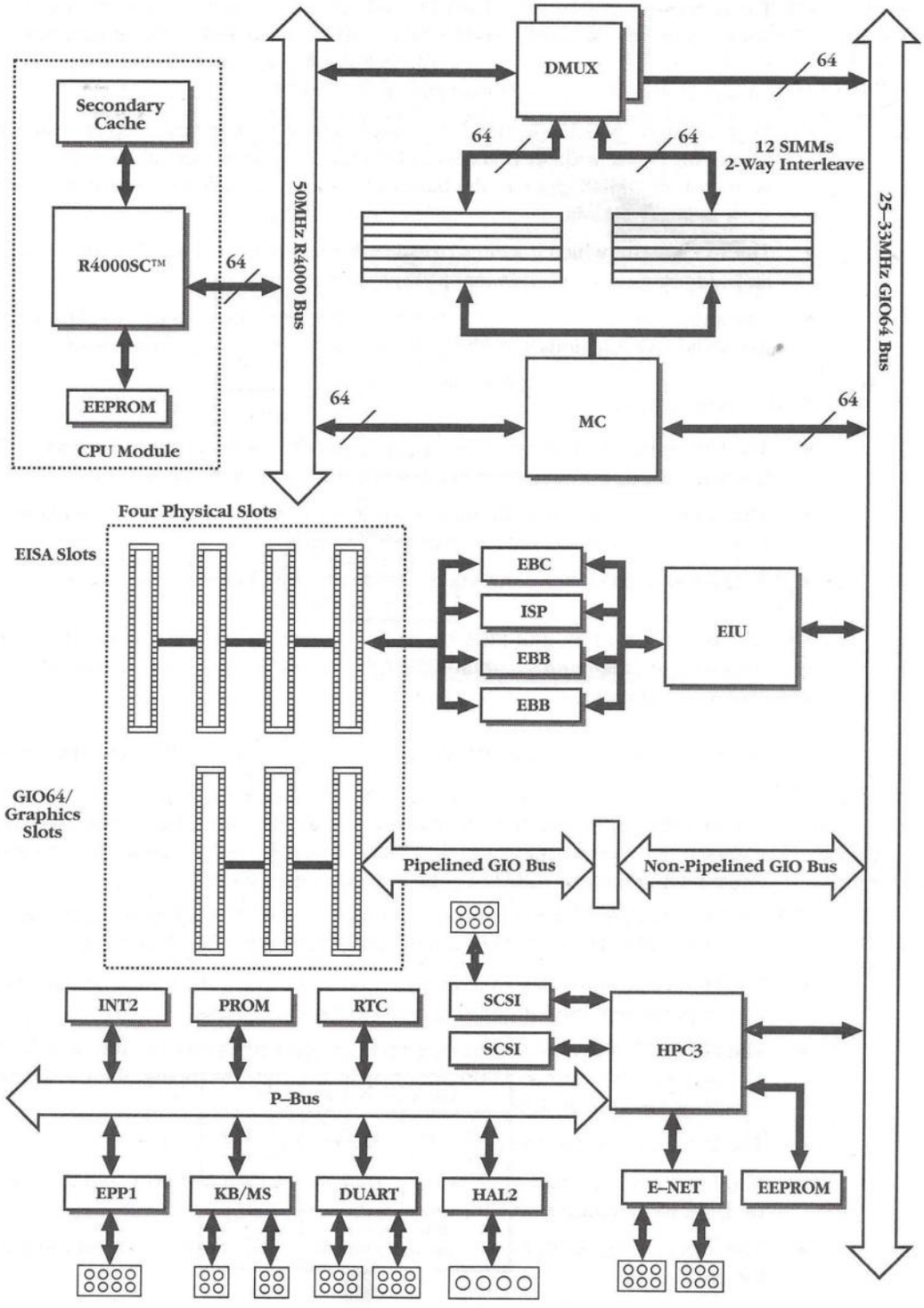


FIGURE 2 R4000SC/R4400SC CPU board.

The R4000SC/R4400SC board contains four functional sections, as illustrated in Figure 15:

- The processor core contains the CPU and secondary cache. This section is designed to take advantage of the R4000SC/R4400SC's increased speed and its 64-bit data bus. The CPU, second-level cache, oscillator, and EEPROM of this section have been separated and mounted on a CPU module for easy replacement.
- Main memory, which contains DRAM and supporting circuitry. This section is also designed to provide 64-bit-wide CPU access to DRAM and implements the memory interleave function with custom DMUX chips in the base CPU board. This allows the use of standard, off-the-shelf memory SIMMs.
- The I/O system, which contains peripheral ports and hardware designed to handle incoming and outgoing data with minimal CPU overhead.
- The audio system, a new audio system architecture which utilizes the HAL2 ASIC to perform the audio I/O functions replacing the need for a digital signal processor.

Three buses connect parts of the CPU board:

- The CPU bus, which connects the CPU module to the bus control hardware. This bus is 64-bits wide to support the R4000SC/R4400SC CPU and its 64 bit datapath.
- The GIO64 bus, which is the main system bus connecting the processor core, main memory, I/O system, expansion slots, and graphics board.
- A 32-bit wide EISA bus connects the GIO64 to the EISA expansion slots.

The CPU bus, GIO64 bus, and EISA bus have separate clocks and run at different speeds so that each part runs at maximum capability; the CPU and other chips can be upgraded independently as technology improves.

Silicon Graphics developed custom ASICs to aid communication between the system and the buses:

- The MC ASIC performs many functions, such as the GIO64 bus arbiter, which provides an interface between the CPU and the GIO64 bus. It is also the memory controller, allowing direct memory access (DMA) by devices other than the CPU.
- DMUX ASICs are data path chips, controlled by the MC chip, that isolate the CPU bus from the GIO64 bus. They also perform the memory interleaving functions.
- The HPC3 ASIC provides an interface to peripheral I/O, the audio system, and other devices on the peripheral bus, connecting them to the GIO64 bus.
- The EIU ASIC provides an interface between the GIO64 bus and the Intel EISA chip set. The EIU performs bus protocol conversion, selective byte swapping, EISA arbitration, and bus throttling for EISA devices.
- The INT2 ASIC is the system timer and interrupt controller chip.
- The EPP1 ASIC is a high-performance, bidirectional parallel port chip that can transfer data by DMA to minimize host CPU interaction.
- The REX or HQ2 ASIC, located on the graphics board, connects the entire graphics board to the GIO64 bus.

3.1 Processor Core

The processor core is centered around the CPU module, which contains the CPU and its secondary cache. The processor core uses three types of custom chips: the MC ASIC to give the CPU access to memory and the GIO64 bus; DMUX ASICs to isolate the CPU bus from the GIO64 bus; and the INT2 ASIC to deliver CPU interrupts.

The MIPS R4000SC CPU is from the MIPS RISC (Reduced Instruction Set Computer) family of microprocessors. This chip (shown in Figure 3) contains the main processor, a floating point processor, an 8-KB onboard instruction cache, and an 8-KB onboard data cache. It also provides a dedicated interface to a 1MB second-level cache. The R4000SC chip's external clock rate is 50 MHz, but it runs internally at 100 MHz. The 64-bit data and instruction paths to the chip's caches bring in data and instructions at a speed which minimizes cache misses and CPU idling. System performance exceeds 85 MIPS (VAX Dhrystone), 16 MFLOPS (double precision), 70 SPECmarks89, 61 SPECfp92, and 57 SPECint92.

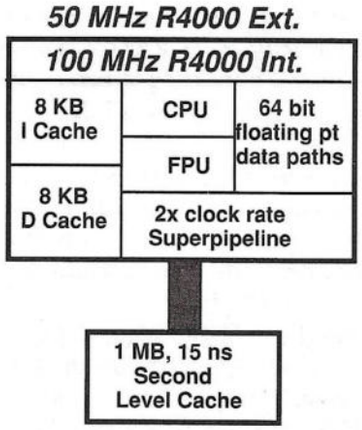


FIGURE 3 The functional sections of the MIPS R4000SC CPU.

The MIPS R4400SC CPU is the most recent addition to the MIPS RISC family of microprocessors. This chip (shown in Figure 4) contains the main processor, a floating point processor, a 16 KB onboard instruction cache, and an 16 KB onboard data cache. Like the R4000SC CPU, the R4400SC CPU also provides a dedicated interface to a 1 MB second-level cache.The R4400SC chip's external clock rate is 75 MHz, but it runs internally at 150 MHz. The 64-bit data and instruction paths to the chip's caches bring in data and instructions at a speed which minimizes cache misses and CPU idling. System performance estimates exceed 120 MIPS (VAX Dhrystone), 22 MFLOPS (double precision), 100 SPECmarks89, 86 SPECfp92, and 82 SPECint92.

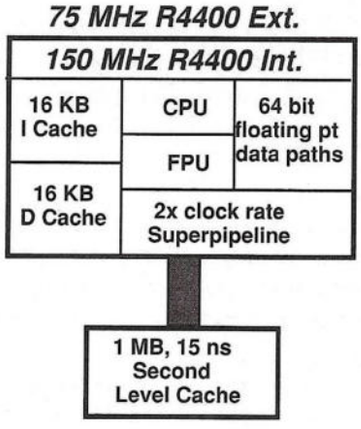


FIGURE 4 The functional sections of the MIPS R4400SC CPU.

Both R4000SC and R4400SC use superpipelining to achieve the fast internal speed. Superpipelining is a variation of pipelining supported by the MIPS R3000A CPU. In normal pipelining, the CPU breaks each instruction into separate one-cycle steps (usually fetch, read, execute, memory, and write back), and then executes instructions at one-cycle intervals. Pipelining allows instructions to overlap, which allows the R3000A CPU to execute close to one instruction per cycle instead of one instruction every five cycles.

At the fast R4000SC/R4400SC CPU clock rate, some instruction steps such as cache reads and writes can't execute in a single pipelined cycle. Superpipelining executes each of these critically slow steps in a single cycle to provide higher throughput. To do so, it first breaks instruction steps into substeps. The substeps are then pipelined in a process separate from standard pipelining, which executes the full step in a single cycle. R4000SC/R4400SC superpipelining is optimized so that it requires little control logic and instruction structure, unlike SuperScaler implementations in chips such as the Intel i860 and the IBM RS/6000 CPUs.

The R4000SC/R4400SC CPU supports both the MIPS I instruction set (used by the R3000A CPU) and the MIPS III instruction set. Data pathways in MIPS III are 64 bits wide, giving the system the ability to load and store full floating point double words in a single machine cycle. The MIPS III instruction set also contains synchronization and advanced cache control primitives.

The CPU Module, which houses the R4000SC/R4400SC CPU, its second-level cache, and an accompanying EEPROM chip, is easily removed from the R4000SC/R4400SC CPU board. It can be replaced with a CPU module containing a faster processor with larger caches as faster CPUs become available. Because the internal CPU clock speed isn't coupled directly to the system bus clock speed, faster CPUs will work effectively in the R4000SC/R4400SC board.

The MC ASIC, the Memory Controller (shown in Figure 5), is a custom Silicon Graphics chip connected to the CPU module by the CPU bus. It's also connected to the GIO64 bus (the system bus), and has address and control lines connected to main memory. It performs many functions:

- It provides an interface between main memory and the CPU core
- It serves as a DMA (Direct Memory Access) controller for all memory requests from the graphics system or any other devices on the GIO64 bus
- It acts as a system arbiter for the GIO64 bus
- It provides single-word accesses for the CPU to GIO64 bus devices and to the graphics system
- It passes on interrupts from the INT2 ASIC to the CPU
- It initializes the R4000SC/R4400SC CPU on powerup, executes CPU requests, refreshes memory, and checks data parity in memory

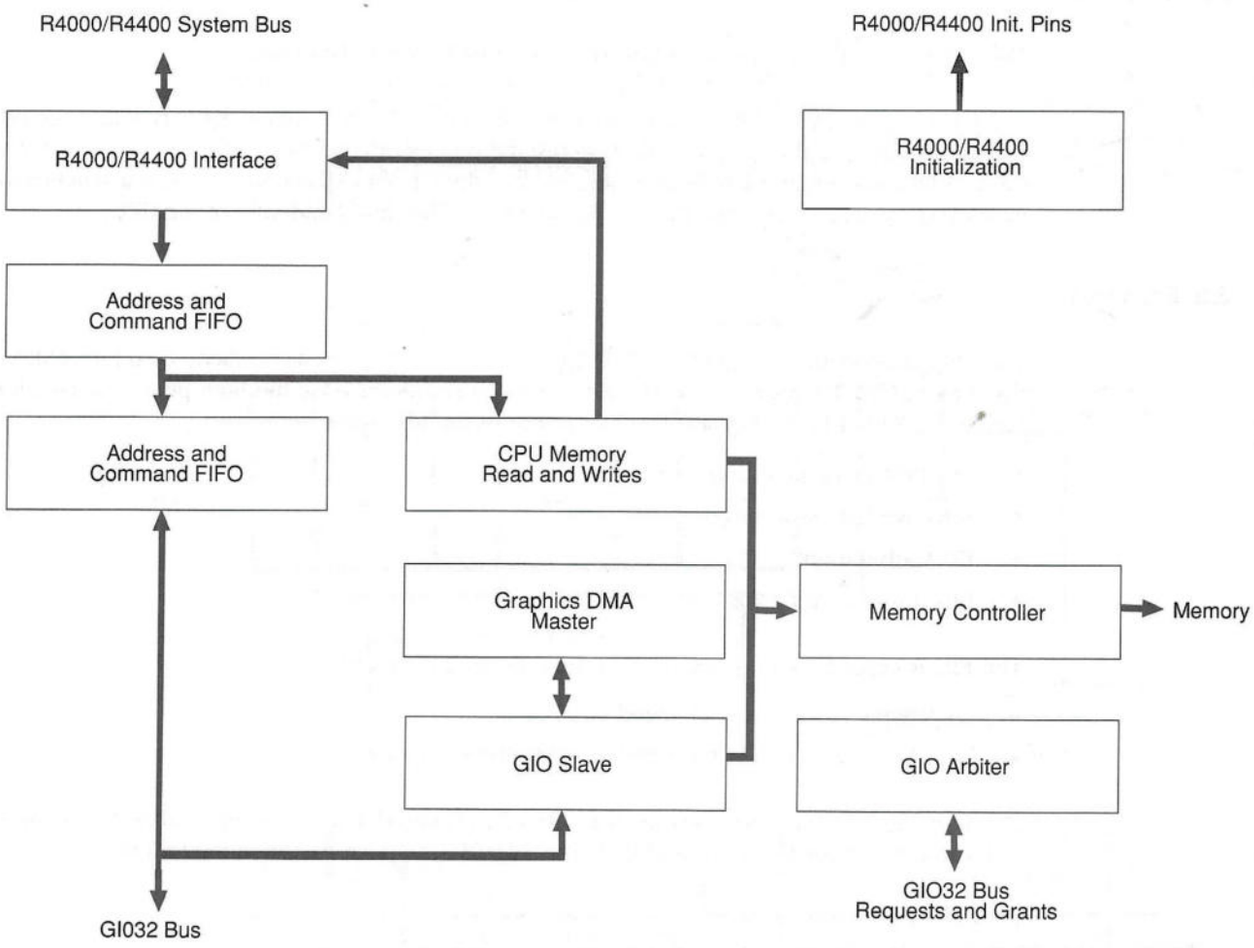


FIGURE 5 A block diagram of the MC ASIC. The MC runs the system bus, handles memory access for CPU and GIO64 devices, works as a DMA controller, and fulfills other miscellaneous functions.

Of special note is the MC's ability to support Virtual DMA requests from processes running on the CPU. The process can also set up a DMA descriptor in MC and then request the DMA engine to start. The memory addresses used in the DMA descriptor are virtual memory addresses which the MC translates (using a TLB and UNIX page tables) to physical memory addresses. When the DMA operation is finished, an interrupt may be generated (if the interrupt is enabled in MC) to inform the CPU.

The DMUX ASICs are a two-chip slice of a data crossbar between the CPU, main memory, and the GIO64 bus. The two DMUX chips are, together, a data path with control signals generated by the MC. They isolate the CPU bus from the memory system and the GIO64 bus. They also contain synchronization FIFOs to perform flow control between the various subsystems, and they interleave main memory to increase peak memory bandwidth.

The INT2 ASIC is connected to the MC chip instead of directly to the CPU. The MC chip passes on all interrupts from INT2 to the CPU.

3.2 GIO64 Bus

The GIO64 bus, the main system bus, provides a 64-bit wide data path.

The GIO64 is the Indigo^2 workstation's main system bus and is designed for very high speed data transfer. It connects the Indigo^2 main systems: the processor core, main memory, the I/O systems, the graphics system, and any boards plugged into the GIO64 expansion slots. It is a synchronous, multiplexed address/data, burst mode bus that is clocked independently of the CPU.

3.3 EISA Bus

The EISA subsystem consists of the EISA Interface Unit (EIU), a custom Silicon Graphics ASIC, and the Intel 82350DT EISA chip set. The EIU provides an interface for the high performance GIO64 bus and the Intel EISA chip set. The EIU performs the following:

- bus protocol conversion
- selective byte swapping
- EISA arbitration
- bus throttling for EISA devices

The EIU is capable of burst transfers at the following data rates:

- 25 MBytes/second at GIO speed of 25 MHz
- 33.3 MBytes/second at GIO speed of 33 MHz

The Intel 82350DT chip set consists of an EISA Bus Controller (EBC), Integrated System Peripheral (ISP), and two EISA Bus Buffers (EBB). The 82350DT chip set performs the following:

EISA Bus Controller

- Support for EISA/ISA memory-i/o cycles
- Supports EISA/ISA wait/no-wait cycles
- Supports EISA Burst cycles
- Generates EISA signals for ISA masters
- Supports Type A,B,C, DMA cycles
- Supports compatible DMA cycles
- Controls EBB during byte assembly/disassembly

Integrated System Peripheral

- Provides Enhanced DMA functions
- Provides EISA Interrupt control
- Provides EISA Counter/Timer
- Provides EISA bus timeout logic

EISA Bus Buffers

- Provides data buffering and swap functions
- Provides address buffering and latch functions

3.4 Main Memory

Main memory, which is controlled by the two DMUX ASICs, provides system access to large amounts of DRAM. Memory consists of standard off-the-shelf 36-bit wide DRAM SIMMs (which must have 80 ns RAS access time and fast page-mode capability). To support the increased bandwidth of the R4000SC/R4400SC CPU, the DMUX chips interleave the SIMMs to create a 64-bit wide two-way interleaved memory system.

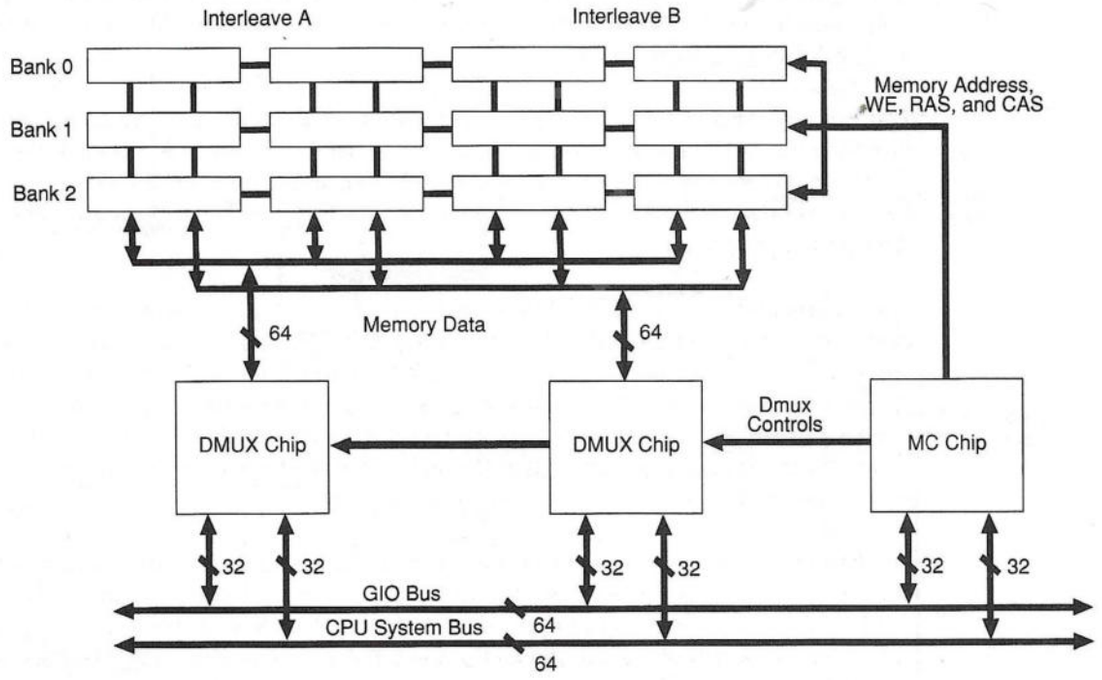


FIGURE 6 Memory on the R4000SC/R4400SC CPU board interleaves SIMM strips in banks of four, and connects them to the CPU and the GIO64 bus with DMUX and MC chips.

Main memory can be configured to be as little as 32 megabytes or as much as 384 megabytes. The R4000SC/R4400SC CPU board has 12 SIMM sockets, arranged in three groups of four. Each socket group must use SIMMs of the same size, but SIMM sizes can differ between groups to allow different memory configurations. Maximum capacity is:

- 96 MB using all 8 MB SIMMs
- 192 MB using all 16MB SIMMs
- 384 MB using all 32 MB SIMMs

3.5 The I/O System

The I/O system ties together a variety of I/O ports and the chips that drive them, a system clock, and the system PROM for booting up. It uses a peripheral bus to transfer some I/O data, and also uses a custom chip—the HPC3 ASIC—to provide an interface between the system and the GIO64 bus.

The HPC3 ASIC, the High Performance Peripheral Controller, is a custom Silicon Graphics chip that connects to the GIO64 bus and directly to several of the I/O ports. It is the heart of the I/O system, and quickly transfers data between main memory and a rich collection of peripheral devices, at the peak rates of such devices. It uses minimum bandwidth on the GIO64 bus, freeing the bus for other data transfers.

The HPC3 permits fast data interchange between peripheral devices and main memory without involving the CPU, improving both CPU and peripheral performance. For each peripheral device, the HPC3 provides an independent FIFO data buffer, and supports DMA to main memory through the GIO64 bus and the MC ASIC. It provides interfaces to the serial ports and other devices through the peripheral bus.

The Ethernet interface consists of both an AUI and a 10BASE-T Ethernet port supported by a controller that is connected directly to the HPC3 ASIC. The interface automatically selects between the AUI and 10Base-T ports; the user does not have to manually change a DIP switch. The HPC3 supplies the logic required to retransmit packets when collisions occur and to manage the interface's 64-byte FIFO buffer. When the HPC3 receives a packet, it interrupts the CPU after it writes the packet into memory. When transmitting, it interrupts the CPU when a packet is successfully sent or when 16 transmission attempts have all failed.

The Fast SCSI-2 interface consists of one internal channel and one external channel. The internal channel connects three internal SCSI devices. The external channel provides an external high-density SCSI port on the rear of the central unit. Each Fast SCSI-2 channel is supported by a SCSI controller connected directly to the HPC3 ASIC. The HPC3 uses two FIFO buffers to enable burst use of the GIO bus.

The parallel port interface provides a bidirectional Centronics parallel port to connect printers, plotters, scanners, and other similar devices. The port is connected to the peripheral bus and provides a FIFO buffer used to transfer data between main memory and the parallel port at up to 1.0 MB/sec.

The peripheral bus (P-Bus) is a 20-bit address, 16-bit data bus used by the HPC3 for additional peripheral support. It connects the boot PROMs, a real-time clock, the timer, two serial ports, a mouse port, a keyboard port, the EPPI ASIC parallel port interface and the audio system through the HAL2 ASIC. There is a 384 byte memory buffer that is shared by all of the peripheral bus devices to buffer DMA transfers to and from memory.

The serial interface consists of two serial ports, controlled by a DUART chip that connects to the Peripheral Bus. They can be configured as EIA-232 standard devices or as external Apple Macintosh compatible connectors that can connect to common Macintosh peripherals such as laser printers and scanners. The serial ports support a transfer rate of up to 38.4 KBaud.

The PS/2 standard keyboard and mouse are controlled by industry-standard hardware and firmware, ensuring compatibility with a wide variety of third party input devices.

3.6 The Audio System

The Indigo^2 audio system shown in Figure 7 is a daughterboard that allows the Indigo^2 to record, process, synthesize and play professional quality signals. The HAL2, a high density ASIC on the audio module, performs the I/O functions, replacing the need for the dedicated digital signal processor found on the IRIS Indigo. The new architecture provides more features, better real-time performance, much higher aggregate data rates, and lower cost, yet retains binary compatibility for application programs through the use of Silicon Graphics Audio Library (AL).

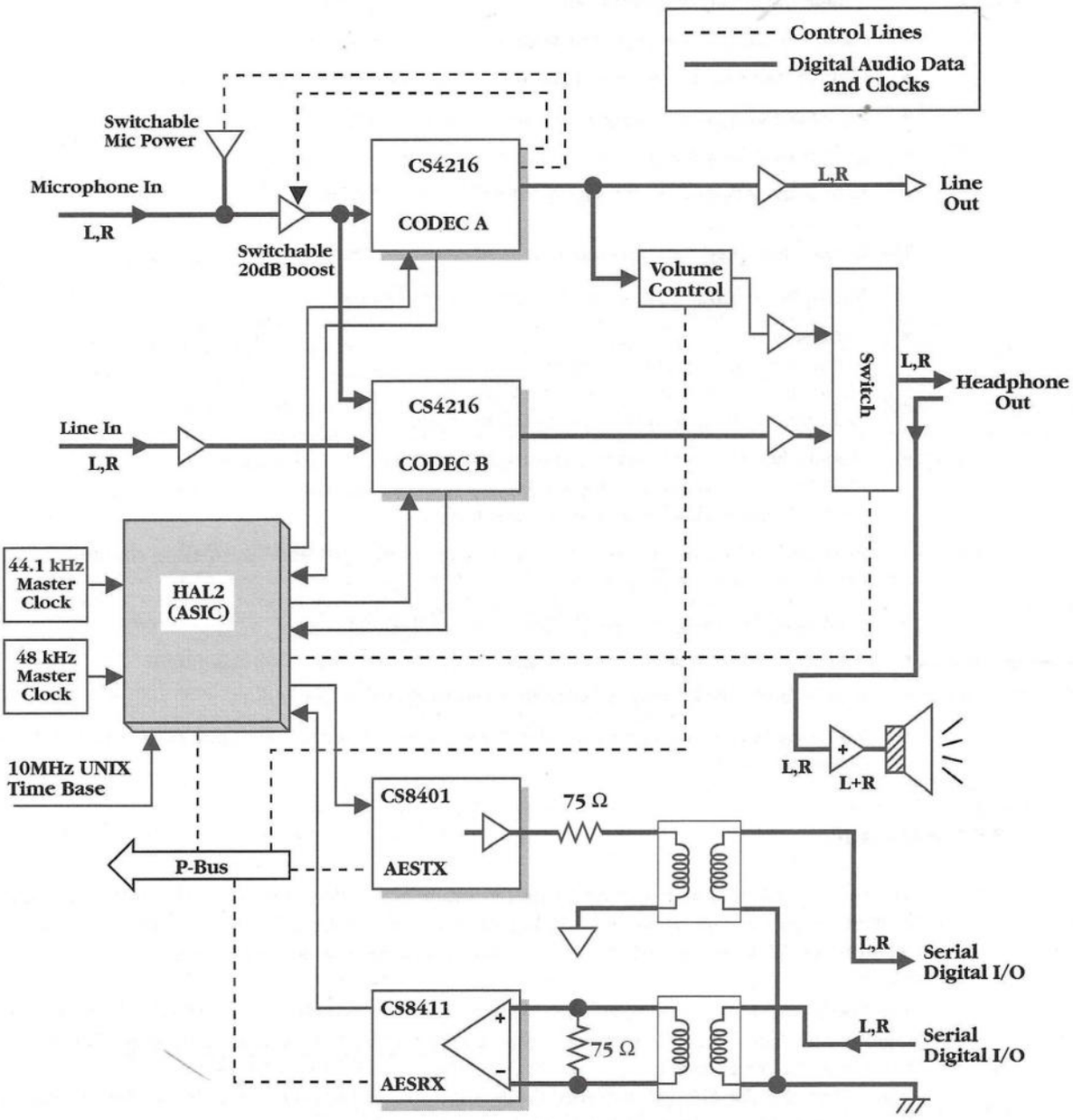


FIGURE 7 Indigo^2 audio block diagram.

The Indigo^2 audio system supports the standard Indigo workstation audio features:

- Stereo line level analog audio input and output
- Stereo headphone output
- Built-in speaker
- AES/EBU digital audio input and output
- Sampling rates of 48 kHz, 44.1 kHz, 32 kHz, 16 kHz, 8 kHz, and more
- Microphone input with DC power
- Simultaneous input and output
- Independent input and output rates
- Output rate may be synchronized to the digital input rate
- Professional quality analog signal processing
- Silicon Graphics Audio Library (AL) API
- Low latency operation for highly interactive applications

The Indigo^2 audio system also introduces several new features:

- Microphone input now supports stereo microphones
- Time-stamped samples
  –utime format time stamps on every sample frame
  –time stamps are synchronized with CPU time base
  –additional bits give resolution to 0.1 microsecond
- Non-audio bit tagging on audio samples
  –left and right analog clip indicator bits
  –P, C, U, and V bits for digital audio samples
- Four channel mode supports four analog channel input and four analog channel output, simultaneously, at full speed
- Analog audio input and serial digital audio input may occur simultaneously
- Analog audio output and serial digital audio output may be independent
- Analog audio input may be synchronized to digital audio input
- Sampling time base is generated by Bresenham's algorithm, allowing near continuous choice of sample rates

3.6.1 HAL2 ASIC

The Indigo^2 audio system is built around a central controller chip, the HAL2 ASIC, two audio CODEC chips, an AES transmitter chip, an AES receiver chip, a microphone input circuit, a headphone/speaker amplifier circuit, and a four-channel-mode output switch.

The HAL2 chip is a 1 micron, 28k gate CMOS gate array which contains the data path and control logic to interface the HPC3 peripheral bus and the audio devices on the module. The major functional blocks connected to the HAL2 are the two CS4216 CODECS, the CS8401 AES transmitter, the CS8411 AES receiver, the headphone and speaker gain circuit, the microphone input circuit, and the four-channel mode output switch.

Notable features of the HAL2 design include:

- Three independent clock generators
  –AES out
  –analog in
  –analog out
- Each of the clock generators can select from three different timebases
- The clock generators use Bresenham's algorithm to scale the input clocks by rational fractions
- The time stamping clock is generated from the same timebase as the unix utime
- Each audio device has its own DMA channel and clock generator
- The DMA channel allocation is configurable in software
- The audio devices attach with conventional 3-wire serial interfaces
- In 4 channel mode, data from all four channels goes over the same DMA channel guaranteeing synchronization

3.6.2 Codecs

The Indigo^2 audio system uses a pair of Crystal Semiconductor CS4216 stereo audio Codecs. These chips are highly integrated monolithic CMOS mixed-signal devices which make use of the latest signal conversion technology. Both the analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are 64x-oversampling delta-sigma 16-bit converters. They also contain on-chip reconstruction and anti-aliasing filters, programmable input gain, and programmable input source switching. The filters' responses track the sampling rate, a significant advantage over the older fixed-response low-pass analog filter designs.

In the normal mode of operation, the Codec A DAC is used for analog output and the Codec B ADC is used for analog input. The Codecs can use independent sample-rate clock generators from the HAL2, so that the analog input sample rate and the analog output sample rate may be selected independently. The analog input (to Codec B) is selectable from either the line or microphone inputs under software control. The analog output signal (from Codec A) is routed both to line-out and to the stereo headphone/internal loudspeaker circuit. The user gets true line-level signal and a volume-adjusted headphone/loudspeaker output.

The Indigo^2 audio system provides an enhanced mode of operation that extends the number of simultaneously active analog input channels from 2 to 4 and the number of simultaneously active analog output channels from 2 to 4.

In 4-channel mode, both Codecs are synchronized to the same sample rate and the Codecs are used simultaneously for input (ADC) and output (DAC). Codec A's input (ADC) comes from the microphone input, Codec B's input (ADC) from the line input. Codec A's output continues to be routed to the line output, but Codec B's output is routed at line-levels to the headphone jack.

3.6.3 Serial Digital Audio Transmitter

The Indigo^2 has an industry-standard, transformer-coupled, serial digital audio output that supports up to 24-bit stereo samples at all available sample clock rates. The audio and non-audio bits may be coded to support both professional and consumer standards (AES3, IEC958).

3.6.4 Serial Digital Audio Receiver

The Indigo^2 has an industry-standard, transformer, coupled, serial digital audio input that supports up to 24-bit stereo samples at up to a 50 kHz sample rate. The sample rate clock recovered from this input may be used to generate synchronized sample clocks for the Codecs and serial digital audio transmitter. All of the bits received in the serial digital channel including U, C, V, and P are input to the computer. Both professional and consumer coding formats are supported by AES3, IEC958.

3.6.5 Microphone

The Indigo^2 comes standard with a high-quality, electret condenser monaural lapel microphone. The microphone is omnidirectional and has both a wide-frequency response and a large dynamic range.

The Indigo^2 microphone input circuit provides DC power for active circuitry in microphones that require it, while retaining compatibility with other types of microphones. Powered microphones, such as the one supplied with Indigo^2, use this DC power to drive a large low-impedance signal back to the audio circuitry, avoiding the problems commonly associated with low-level microphone signals and electrically noisy computer environments.

The microphone input circuit accepts both monaural and stereo microphones. In addition to the input source switching and software-controlled gain functions available in the Codecs, the DC power feature and a hardware 20 dB gain stage may be enabled and disabled via software control.

3.6.6 Internal Speaker

The internal speaker in the Indigo^2 audio system outputs the sum of the left and right line-out channels. The speaker is shielded to protect the graphics and video monitors from the speaker's magnetic field. Speaker volume is software controlled.

3.6.7 Headphone Output

The Indigo^2 audio system provides a stereo headphone output connection, suitable for connecting standard headphones without need for external amplifiers.The headphone volume for each channel is software controlled. When a headphone is plugged into the connector, the internal speaker is automatically disconnected.

3.7 Expansion Slots

The Indigo^2 has four expansion slots; all four slots have EISA bus connectors, three of the slots have GIO64 pipelined bus connectors as well. The EISA bus fully conforms to version 3.12 of the EISA standard, allowing the use of a large variety of EISA and ISA components.

Section 4 XL Graphics

XL Graphics, the Indigo^2 entry graphics subsystem, uses the CPU to implement the IRIS Graphics Library application programming interface rather than having a dedicated Geometry Engine. XL Graphics, shown in block diagram in Figure 8, provides high resolution, full 24-bit color and includes the following:

- the Raster Engine (REX3) ASIC, which converts geometric data processed by the CPU into pixel and line data that it then writes into the framebuffer
- the framebuffer (VRAM), which contains the pixel color and overlay data for the 1280x1024 display, and the CID planes for arbitrary window clipping operations
- the VC2 (video controller) ASIC, XMAP9 ASIC, and CMAP which, together with a 24-bit DAC, generate the RGB video signals sent to the monitor

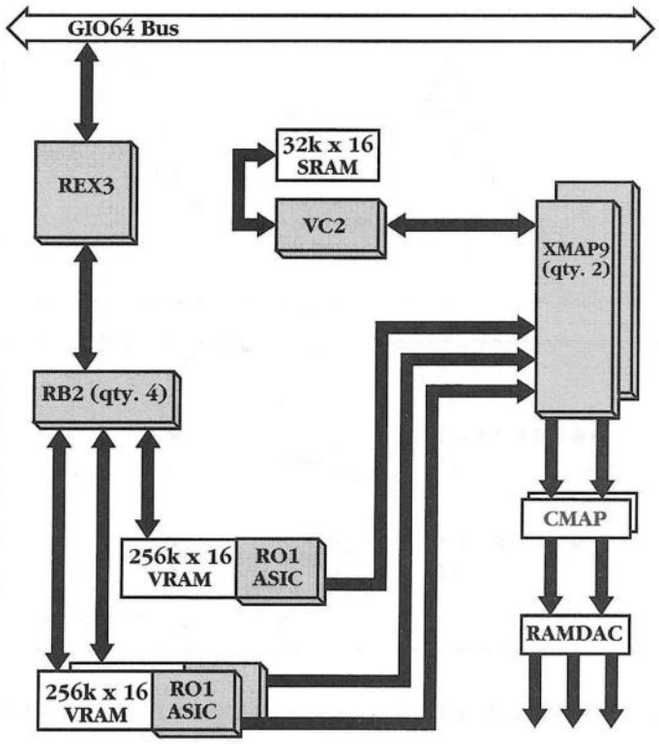


FIGURE 8 The XL Graphics Board. The shaded boxes show Silicon Graphics-designed ASICs.

The main bus on the XL Graphics board provides a communication path between the elements of the graphics subsystem. The XL Graphics board is connected to the GIO64 bus via the REX3 ASIC, which can access data from the CPU at a burst rate of 267 MBytes per second.

4.1 Graphics Processing

XL Graphics makes extensive use of the power of the R4000/R4400 CPU by implementing the IRIS Graphics Library™ application programming interface as a set of highly efficient software algorithms. Because of the flexibility inherent in the software-based IRIS GL™ implementation, new graphics functions can be added as new software releases, without the need for costly hardware upgrades.

The CPU uses the IRIS GL to transform three-dimensional polygons to 2D screen coordinates, decompose them into triangles, and finally decompose the triangles into spans by exact point sampling of the triangle's interior. These spans are then passed on to the REX3 ASIC, which interpolates them and renders the results into the framebuffer.

Figure 9 shows how 3D polygons are processed by the CPU and the REX3 ASIC. All transformation, clipping, and lighting calculations for points, lines, and polygons are performed in software by the CPU, including Z-buffer calculations, which are implemented in 32-bit resolution without the use of dedicated Z-buffer bitplanes.

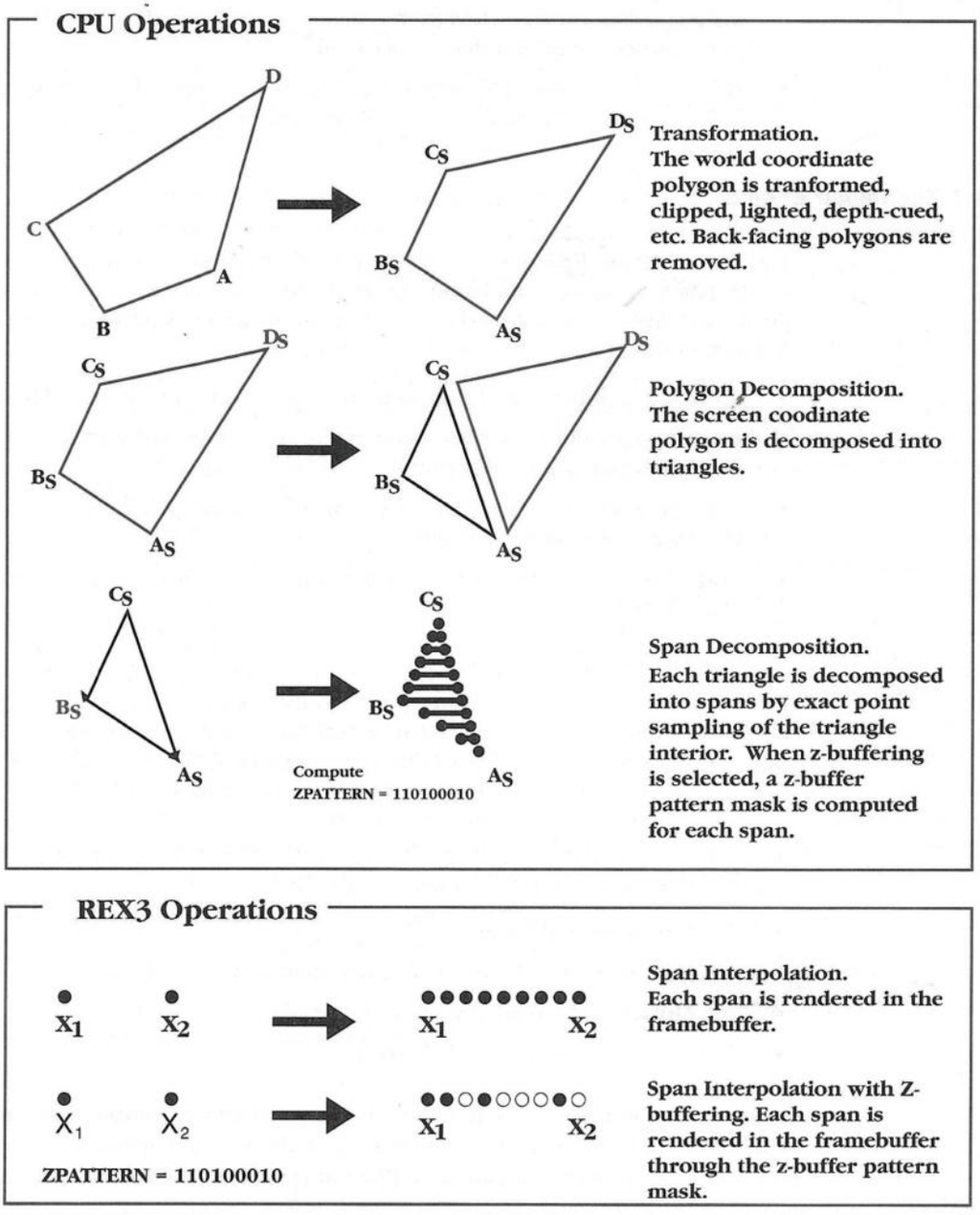

CPU Operations
D
C
A
B
DS
CS
BS
AS
Transformation.
The world coordinate polygon is tranformed, clipped, lighted, depth-cued, etc. Back-facing polygons are removed.
Polygon Decomposition.
The screen coodinate polygon is decomposed into triangles.
Span Decomposition.
Each triangle is decomposed into spans by exact point sampling of the triangle interior. When z-buffering is selected, a z-buffer pattern mask is computed for each span.
Compute
ZPATTERN = 110100010
REX3 Operations
X1
X2
Span Interpolation.
Each span is rendered in the framebuffer.
Span Interpolation with Z-buffering. Each span is rendered in the framebuffer through the z-buffer pattern mask.
ZPATTERN = 110100010

FIGURE 9 XL Graphics processing. The majority of XL Graphics computation is performed in software by the CPU.

XL Graphics offers several advantages in speed and flexibility over hardware-based graphics systems:

- IRIS® Advanced Graphics functionality such as antialiased lines and polygons and exact point sampling is provided.
- Character (font) rendering is performed by the CPU, unencumbered by unnecessary filtering through graphics hardware.

- 2D rendering is optimized in software with algorithms that speed computation by eliminating the z coordinate parameters from calculations performed by the CPU, resulting in very high performance for 2D graphics applications.
- Because XL Graphics performance is directly proportional to CPU speed, upgrades to faster CPUs automatically increase application performance.

4.2 The Raster Engine

The Raster Engine (REX3) is a pipelined, pixel-filling, and line-drawing ASIC which provides pixel shade, pattern, logicop, and blend operations for point, span, block, and integer or subpixel positioned line addressing modes. The REX3 ASIC achieves outstanding performance by the following techniques:

- buffering multiple graphics drawing requests in an on-chip input FIFO
- overlapping memory accesses, command executions, and command setups to achieve maximum pipeline throughput
- using page-mode accesses in the VRAMs when appropriate, because pixels in the same page can be accessed more quickly
- buffering multiple display bus (VC2, XMAP9, CMAP, RAMDAC, etc.) requests in a second, on-chip FIFO

The REX3 has five basic drawing primitives: point, line, span, block, and screen-to-screen copy. Draw commands can modify either pixel, overlay, or CID planes. The REX3 hardware recognizes a total X11 pixel address space of 64K x 64K pixels or a GL pixel address space of 4096 x 4096 pixels including 64 x 1K pixels of offscreen memory. REX3 can read pixel, overlay, pop-up, or CID information from both onscreen and offscreen memory.

REX3 supports both flat and linear (Gouraud) shading in both color index and RGB formats with optional dithering. The peak fill rates for the REX3 are:

- 20 Mpixels/second for lines
- 400 Mpixels/second for clear (flat, undithered, and unstippled)
- 100 Mpixels/second for flat spans (dithered)
- 50 Mpixels/second for shaded spans

Dithering is window-relative in REX3, in contrast to the screen-relative dithering supplied in other GL™ implementations. This has the benefit of allowing a window to be moved while it is rendering, without creating artifacts. REX3 also includes the following features:

- It provides a window offset register, which holds the window origin and allows pixel addresses within a window to be stored relative to the origin.
- It maintains five screen masks. One of the screen masks is mapped into the user address space and can be set and used by calls in the IRIS Graphics Library application programming interface (API). The other four are available to the window manager to facilitate the clipping of overlapping windows. The addition of CID planes allows non-rectangular window clipping.
- It implements a set of sixteen logic operations on writes into the framebuffer. Window managers can use these functions to highlight selected areas and objects, to remove an object without removing objects in front or back of it, etc.

- It uses a screen to screen block move with logic op function, making movement of windows a quick and straightforward process.
- It considers the upper left corner of the screen to be the viewable origin, which supports X11 protocol screen addressing. A programmable register mode can be used to define the lower left corner as the viewable origin for GL.

In addition to features that support windowing, REX3 also has features to support IRIS GL and X11 library functions. These include:

- Bresenham's line drawing (including fractional-positioned, endpoint filtered antialiased lines).
- Two 32-bit recirculating pattern/stipple registers, which hold values that either prohibit the filling of a pixel (transparent stippling) or choose between the foreground and background color (opaque stippling). One register is of programmable length for X11 graphics and allows a repeat count for GL graphics; the other is 32-bit fixed length, and is useful for Z-buffering when in transparent mode. Both registers can be selectively enabled, allowing them to be used alone or in tandem.
- Burst-mode GIO64 bus transfers. When the GIO64 bus is operating in burst-mode, 8 bytes are transferred every cycle for a peak rate of 267 MBytes per second. REX3 can accept data into its FIFO at this rate, although processing the data takes longer. REX3 reads or writes pixel data over the GIO64 bus into a rectangular area at 43 million pixels per second. Both REX3 and MC1 support a robust rectangular DMA function that allows pixel data to be aligned to any arbitrary byte address and to have an arbitrary byte stride between scanlines.
- Commands for drawing IRIS GL color index and RGB antialiased lines. For color index lines, REX3 can perform a color comparison test for each pixel for full support of the IRIS GL API's zsource (ZSRCCOLOR) mode. This technique is useful when depthcueing or anti-aliasing because it can prevent darker pixels from drawing over brighter pixels, such as in the case of a dark background. For RGB lines using the GL blendfunction to enable alpha-blending, REX3 computes alpha based on line coverage.
- 20-bit iterators for each of red, green, and blue to guarantee accurate color interpolation. This assures that accumulated color interpolation error is not visible on the screen. In addition, one of the 20 bits is used as an overflow/underflow bit to clamp invalid colors to either all zeros or all ones. Color index mode is supported by a 24-bit iterator in order to maintain accuracy for 12-bit pixels in color index mode.

4.3 Framebuffer and Clipping Planes

There are four kinds of bitplanes in the XL Graphics subsystem: pixel, pop-ups, overlay, and clipping ID (CID) planes. The four bitplanes are implemented as a framebuffer in a 12x256Kx16 bank of VRAM.

Pixel planes hold 24 bits of information for each pixel of the display. In single buffer mode, the framebuffer contains a 12-bit color index or 24-bit RGB (8 bits each for red, green, and blue).

Pop-up planes, holding 2 bits per pixel, are used for pop-up menus, dialog boxes, and other components of a graphical user interface that temporarily obscure the image.

Clipping ID planes, also holding 2 bits per pixel, store information about which parts of windows are visible on the display. Multiple windows can overlap each other, totally or partially obscuring their contents. Individual pixels can be masked against a window boundary, thereby supporting non-rectangular windows without imposing additional overhead on the window system. The clipping ID (CID) planes are in the framebuffer VRAM.

The overlay planes on XL Graphics hold 8 bits per pixel.

The framebuffer is connected to the REX3 ASIC via the RB2s. Full use of the VRAM bandwidth is realized through a 128 pixel wide data path that connects the framebuffer to the RB2 ASIC. The framebuffer displays to a 1024 x 768 or 1280 x 1024 pixel monitor.

4.4 Color Lookup

The display of pixel data is controlled by the VC2 ASIC. It determines the timing of transfer cycles performed by the REX3. The serial VRAM data is buffered in the RO1 ASICs and then sent at half video rate to a pair of XMAP9 ASICs. The XMAP9 ASICs format the lookup index on a per-window basis as instructed by the VC2 for both color index and RGB modes, double-buffering, pixel depths, a pop-up cursor, and overlay planes.

Depending on the mode, each pixel to be displayed is formatted with an offset of n x 256 in order to index the desired section of the CMAP RAM as shown in Figure 10. This resulting lookup index is passed to the CMAP ASICs which generate 24-bit RGB values for display. These values finally enter the RAMDAC where they are gamma-corrected for the monitor by the use of a second level of lookup tables, and analog RGB output is produced.

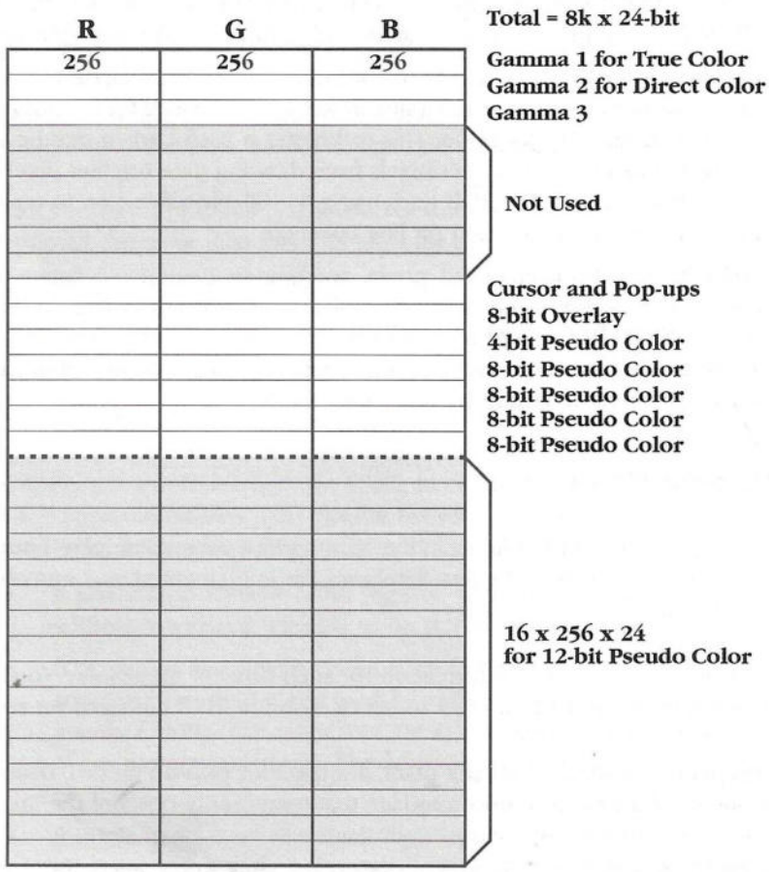


FIGURE 10 Organization of the CMAP RAM (indexed by row).

Section 5 XZ and Extreme Graphics

XZ and Extreme Graphics subsystems provide an unprecedented level of graphics price/performance because of breakthroughs in three critical areas: VLSI design, graphics architecture, and electronics packaging.

XZ Graphics includes two Geometry Engine processors, a raster engine, high resolution full 24-bit color, and a built-in 24-bit Z-buffer.

Extreme Graphics includes eight Geometry Engine processors, two raster engines, high resolution 24-bit color, and a 24-bit Z-buffer.

5.1 Features

Both XZ and Extreme Graphics have the following features:

- 24-bit color
- 24-bit Z-buffer
- 4 stencil bitplanes
- 4 Overlay and 4 Window Clipping ID planes
- 32 simultaneous window modes
- 1280 x 1024 screen resolution
- Screen refresh rate at 60 Hz and 72 Hz
- NTSC and PAL unencoded video output timings
- Genlock capability
- Stereo viewer control
- Slot for live video I/O option card

Advanced graphics features include hardware support for:

- Subpixel positioning
- Advanced lighting models:
  - Multiple colored light sources (up to 8)
  - Ambient, diffuse, and specular lighting models
  - Phong lighting
  - Spotlights
  - Local and infinite light source positioning
  - Two-sided lighting
- Anti-aliased lines and points
- Full scene anti-aliasing
- High-speed graphics DMA
- Pan and zoom capabilities
- Atmospheric effects

- Sphere rendering
- Pixel-blending capabilities for transparency effects
- Soft shadows and depth-of-field
- Texture-mapping
- Multimode windowing environment
- X11 drawing primitives and pixel move operations
- Non-Uniform Rational B-Spline (NURBS) surfaces

5.2 VLSI Integration

The heart of the XZ and Extreme Graphics subsystems is based on seven custom VLSI designs. Extreme Graphics achieve a 15-fold increase in the level of integration over Silicon Graphics' previous graphics architectures.

Among the most significant new VLSI designs are:

GE7	The Geometry Engine® processor combines standard cell and gate array design with the equivalent of 80,000 custom gates. It features a floating point core surrounded by special circuitry for fast geometry calculations.
RE3	The Raster Engine holds 100,000 custom gates and runs at 50 MHz.
HQ2	The HQ2 is an 80,000 gate control-oriented device that incorporates several different subsystems and clock rates with speeds up to 25 MHz.
VC1	The VC1 is a 50,000 gate control logic design that provides video timing control for the output monitor, run-length encoded windowing tables, and the cursor.
ZRB1	A 13,000 gate device running at 50 MHz that provides Z-buffer I/F.
RB1	A 2,000 gate device running at 50 MHz that provides Z-buffer and framebuffer I/F.
XMAP7	An 18,000 gate device running at 25 MHz that provides pixel formatting and LUT access.

X–Class and E–Class Graphics were developed using a hierarchical top-down design approach that allows simulation at the behavioral, functional, and gate levels. In-depth simulation of the overall design throughout the construction allowed the design team to put together this complex system.

5.3 Graphics Architecture

The Geometry Engine processor (GE7™), the heart of X–Class and E–Class Graphics, was designed with a general purpose microprogrammed floating point datapath architecture. This allows flexible implementation of a variety of algorithms. Added to the general purpose floating point core are many features that ensure high execution efficiency for graphics-related algorithms. The design team paid special attention to internal busing structures, to data stores for variables and intermediate results, and to the construction of the microprogram word. These features result in outstanding GE7 performance for graphics operations.

Multiprocessing in the Geometry Subsystem helps satisfy the heavy computational demands of graphics rendering. Extreme Graphics features eight GE7s, arranged in a unique Single Instruction Multiple Data (SIMD) parallel processing structure for an unprecedented 3D graphics price performance ratio.

Every instruction issues separate graphics primitives to each Geometry Engine processor, allowing all the Geometry Engines to execute the same instruction in one clock cycle. The custom GE7 design includes several special solutions for the SIMD architectural problem. Extreme Graphics goes even further by providing eight Geometry Engine processors in the same parallel processing structure

The custom Raster Engine uses the maximum available bandwidth of today's video RAMs to achieve exceptional framebuffer fill rates for all fill modes. The Raster Engine achieves these fill rates while implementing advanced fill mode features such as Z-buffering, depth-cueing, alpha-blending, raster-ops, dithering, stenciling, clipping region checks, and special effects useful in visual simulation. XZ Graphics provide a single Raster Engine while Extreme Graphics provide two.

For a single RE chip to match the available video RAM bandwidth, the design requires very high clocking rates and multiple pipeline levels. The architecture is based on a variable depth pipeline, which swings from 25 pipe stages up to a depth of 40 stages. Each pipe stage involves carefully tuned arithmetic units, and the whole engine is directed by a carefully constructed pipeline control mechanism.

The image Z values are stored in a separate Z-buffer memory outside the framebuffer video RAMs that hold color values. In order to achieve the same fill rates for Z-Buffered applications and non Z-Buffered applications, the Z-buffer is designed with twice the memory bandwidth of the framebuffer. Both buffers are controlled by the RE3.

5.4 The CPU Interface

Indigo^2 is a 32 bit device on the GIO64 bus. The GIO64 bus provides full-speed burst modes that allow close to maximum use of the bus bandwidth. The CPU main memory has sufficient bandwidth to feed to the GIO buses. The combination of a high bandwidth system bus and high bandwidth main memory is essential to both CPU and graphics performance.

To make use of the data bandwidth available from the CPU, the X–Class and E–Class Graphics architecture includes a set of high-speed DMA data funnels. The DMA data funnels provide a direct connection between the CPU main memory and the graphics frame and Z-buffers. These funnels can transfer a 32-bit word to or from the graphics buffers at a rate of one word per Raster Engine clock. These powerful pixel transfer rates are excellent for applications such as image processing, paint applications, and desktop publishing, as well as processing user data from a GIO64 board slot. DMA data funnels are also implemented within the graphics system to support operations such as bit-BLTing and fast background patterning.

5.5 Packaging

X–Class and E–Class Graphics are largely made up of custom ASICs and readily available commercial memory. Proprietary VLSI design allowed for the removal of most other commercial parts. The result is a compact, low-power, reliable design that achieves high manufacturing yields.

The system employs the latest techniques in surface mount packaging (SMT) and distributes the large number of gates across the seven custom ASICs. The SMT assembly is the current state-of-the-art in reliable, high-yield manufacturing.

Extreme Graphics employs MultiClip Module (MCM) technology to provide a very compact geometry subsystem.

Each board is manufactured to specific tolerances to control the impedance characteristics of the signal traces. This provides an environment where transmission line effects on traces can be controlled, and the integrity of inter-chip signals cans be maintained to a high standard. This is also critical to reliability and high-yield manufacturing.

X–Class and E–Class Graphics are comprised of daughterboards that plug into a base motherboard. This approach has two advantages. First, it is essential to the compactness of the board design. Second, the partitioning allows very high speed critical bus lengths to be kept very short, making significant contributions to manufacturing yield and reliability.

5.6 Graphics Hardware

The X–Class and E–Class Graphics architecture provides an order-of-magnitude leap in graphics processing power over the highest performing workstations currently available in the same price class. The tremendous interactive visual realism enabled by X–Class and E–Class Graphics derives from a unique architecture implemented in 7 custom ASICs designed by Silicon Graphics.

The RISC-based Indigo^2 host CPU provides the graphics subsystem with the description of 2D and 3D objects. This takes the form of IRIS Graphics Library™ commands bundled with world coordinate data. Described are the object's geometric position with respect to the viewer, together with various light sources, color, surface properties, and surface normal vectors used for complex lighting calculations. The X–Class and E–Class Graphics architecture performs transformations and other graphics operations to calculate specific pixel values for each of the 1.3 million pixels on the 1280 x 1024 high-resolution display. Visual data from the RISC host is processed through five pipelined graphics subsystems before being displayed on the screen. These include:

- Command Engine
- Geometry Subsystem
- Raster Engine
- Framebuffer
- Display Subsystem

5.6.1 Command Engine

X–Class and E–Class Graphics are connected to the CPU subsystem via the GIO64 bus. Drawing commands, in conjunction with world coordinate geometric data, are passed across the GIO64 bus and written into the graphics input FIFO. The graphics FIFO buffers differences in computation latencies between the CPU-based application program and the Graphics Engines. The FIFO is implemented as a sub-block inside the HQ2 chip.

The Command Engine (CE) monitors the output of the graphics FIFO and passes the stream of commands and data sent down by the application program to the Geometry Subsystem. The CE analyzes the command stream to determine the types of graphical primitives being received and to uncover the boundaries between these primitives. Based on the results of the analysis, the Command Engine delegates primitives to the Geometry Engine processor(s). The data is read from the FIFO and passed to the delegated Geometry Engine. The Command Engine fills in any graphical parameters not supplied by the user from the state variables specified by earlier subroutine calls, and outputs a complete packet of parameters to the Geometry Engine. The Command Engine accepts coordinate data from the CPU in four formats:

- 16-bit integer
- 24-bit integer
- 32-bit IEEE floating point
- 64-bit IEEE floating point

Color data is also accepted in packed byte format. The Command Engine converts all incoming data words to a uniform floating point format regardless of the input data representation. The Command Engine is implemented as a microprogrammed processor running inside the HQ2 chip.

Figure 11 illustrates XZ Graphics in a block diagram. Figure 12 illustrates Extreme Graphics in a block diagram.

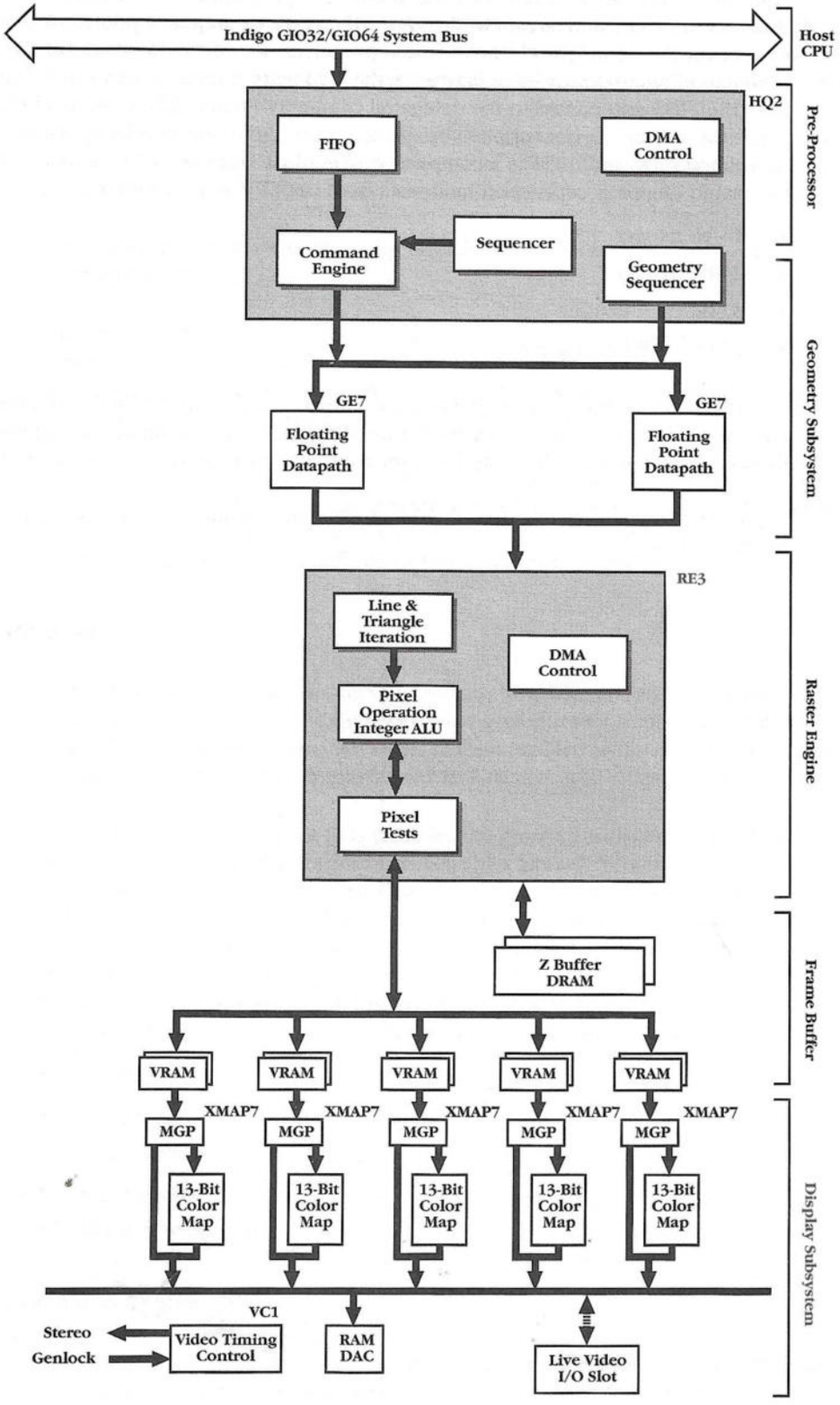


FIGURE 11 XZ Graphics block diagram.

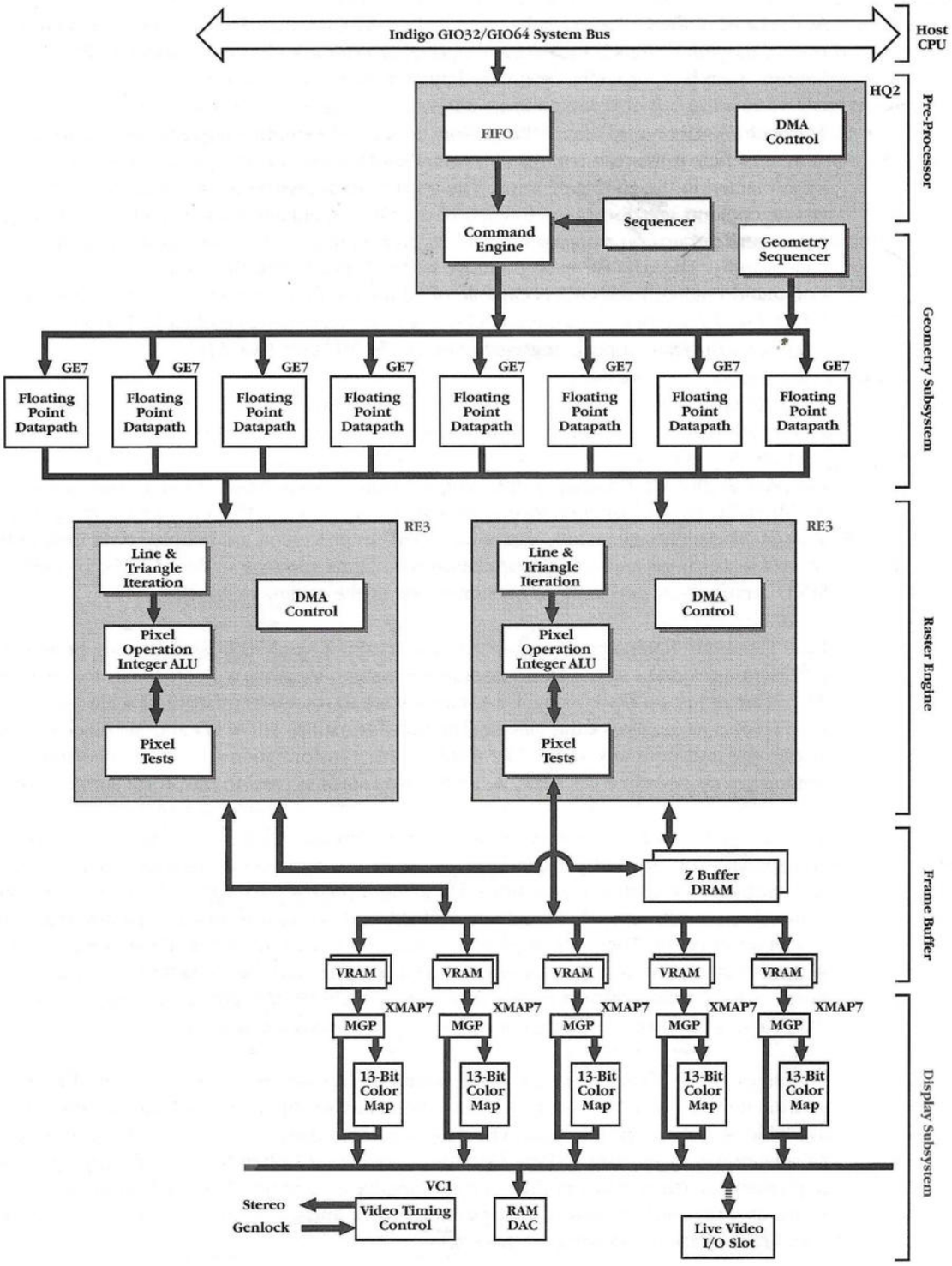


FIGURE 12 Extreme Graphics block diagram.

5.6.2 Geometry Subsystem

At the heart of the Geometry Subsystem is the GE7 Geometry Engine processor, a custom floating point data path designed by Silicon Graphics. XZ Graphics has two Geometry Engine processors. Extreme Graphics has eight Geometry Engine processors

The multiple Geometry Engine Processors of XZ and Extreme Graphics execute together as a SIMD machine under the control of a centralized sequencer. The geometry sequencer is implemented in the HQ2 gate array. The sequencer addresses a wide microinstruction memory whose contents are distributed to each of the GE7s simultaneously. Each Geometry Engine processor operates on a separate primitive, with multiple GE7s operating on the primitives concurrently. The data for each primitive is distributed to the Geometry Engine processor by the Command Engine. Each GE7 is capable of 32 million floating point operations per second (MFLOPS). XZ Graphics can thereby obtain a peak aggregate rate of 64 MFLOPS (4 x 32). Extreme Graphics can obtain a peak aggregate rate of 256 MFLOPS (8 x 32).

The GE7 core is structured to be a general-purpose floating-point data path. There is a short computation latency for maximum throughput efficiency. Two separate arithmetic blocks, one multiply and one add, operate in parallel to achieve the 32 MFLOPS rate. This general-purpose datapath is enhanced with special busing structures into and out of the arithmetic blocks. Additionally, the inclusion of several data stores ensures quick operand retrieval and result storage. These enhancements, useful on a GE7 uniprocessor, are coupled with unique flow of control instructions and data manipulation paradigms allowing multiple GE7s to operate in a SIMD arrangement and achieve maximum use of the arithmetic blocks.

Each Geometry Engine processor receives a stream of single-precision floating point data words representing vertices in the world coordinate system, together with attributes for each vertex. Transformations are done using 4 x 4 matrix stack to rotate, translate, and scale incoming vertices with respect to the eye of the viewer. The transformations allow 2D and 3D objects to be viewed at any size and from any angle. The result of the transformation is a set of coordinates in a homogeneous coordinate system. A 3 x 3 matrix stack is used to transform surface normals.

The next task is to light vertices to improve the viewing and understanding of surface contours and shapes. The Geometry Engine processors maintain the position, direction, and intensity specifications for lighting calculations. Up to eight point-source lights or spotlights are supported. Material specifications include ambient, diffuse, and specular reflectance parameters, and lighting model information. The color applied to each vertex is a function of the vertex position, the surface normal direction, the lighting model, the lights, and the characteristics of the surface. The result of the lighting calculation is either a set of eight-bit red, green, blue and alpha values (in RGB mode) or a single 12-bit color index (in color index mode).

Primitives are then clipped to a 6-plane bounding box describing what region of homogenous coordinate space is visible to the viewer. The ability to clip against additional arbitrary planes is available. A fast accept/reject clip-checking algorithm eliminates the need for complex clipping calculations in most cases. When clipping is required, a Cohen-Sutherland clipping algorithm is implemented. The vertices of the clipped primitive data go through a perspective division that provides a perspective view of the resulting object, and compresses the 3D object into a 2D coordinate space for viewing on the screen.

Polygon decomposition in screen coordinate space comes next. All polygons with four or more vertices are broken into multiple independent triangular pieces. The triangles are then handled identically through the remaining graphics pipelines.

The final stage of calculation in the geometry subsystem is to determine a number of parameters pertaining to the triangle or vector. These parameters are used by the raster subsystem to iterate pixels. They include the bottom most pixel center of the triangle, the triangle-edge slopes, and the parameter slopes in both the X and Y directions. Floating-point precision is used to maintain coordinate integrity when calculating slopes. All color and depth components are first corrected to an initial pixel center. As a result, values iterated in the raster subsystem remain planar across polygonal surfaces, and subsequent Z-buffer calculations result in clean intersections. Furthermore, maintaining fractional X and Y position information for all primitives enables correct multi-pass jittering operations.

Each GE7 passes the resulting parameters set to the Raster Subsystem for iteration.

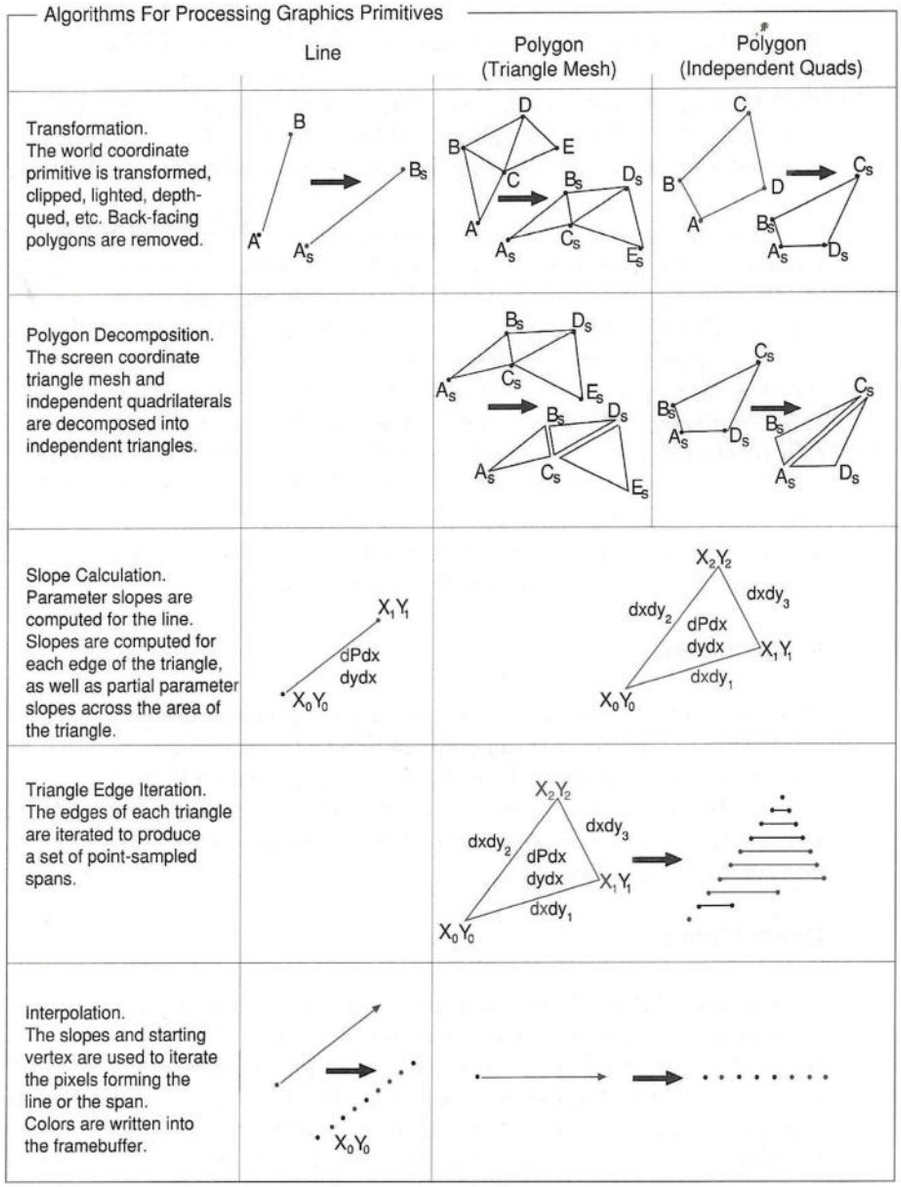

Algorithms For Processing Graphics Primitives
Line
Polygon (Triangle Mesh)
Polygon (Independent Quads)
Transformation. The world coordinate primitive is transformed, clipped, lighted, depth-qued, etc. Back-facing polygons are removed.
Polygon Decomposition. The screen coordinate triangle mesh and independent quadrilaterals are decomposed into independent triangles.
Slope Calculation. Parameter slopes are computed for the line. Slopes are computed for each edge of the triangle, as well as partial parameter slopes across the area of the triangle.
Triangle Edge Iteration. The edges of each triangle are iterated to produce a set of point-sampled spans.
Interpolation. The slopes and starting vertex are used to iterate the pixels forming the line or the span. Colors are written into the framebuffer.
dPdx
dydx
dxdy1
dxdy2
dxdy3

FIGURE 13 Algorithms for processing graphics primitives.

5.6.3 Raster Subsystem

The Raster Subsystem performs the operations required to reduce a vector or triangle description down to the individual pixels to be written into the framebuffer. The core of the raster subsystem is Silicon Graphics' third-generation Raster Engine, the RE3 chip. The RE3 accepts initial pixel values and parameter slopes from the geometry subsystem and iterates either a vector or a triangle. XZ Graphics have a single Raster Engine, Extreme Graphics have two.

The RE3 has a deep and variable length pipeline that swings between 25 and 40 stages depending on the mode of operation. At the front end of the pipeline is a set of DDAs that allow iteration of the various slopes and pixel values initially loaded by the geometry subsystem. The iteration block traverses the line or triangle primitive in full-pixel steps, turning the primitive into an array of pixel values to be sent to the next block.

The pixel operations block has several possible functions. If either pixel blending or raster operations is enabled, this block reads the destination pixel value at the address of the incoming pixel from the iteration block, and performs the appropriate arithmetic or logical merging of the two values. For color index anti-aliased lines, color compare is performed. Fog and haze attenuation is calculated. Pixel values may be dithered before sending to the next block.

The pixel-update-test block determines whether or not a calculated pixel should indeed be written into the framebuffer or Z-buffer. Four simultaneous tests are performed: screen mask check, clipping ID check, Z compare checks, and stencil value check. The pixel address is tested against two screen masks, each of which provide window clipping for any arrangement of two overlapping rectangular windows. If more complex windowing arrangements are encountered, the clipping ID planes are used to check clipping ID. The operation of the clipping ID planes, the Z-buffer planes, and the stencil planes are described in more detail elsewhere in this report. If all four pixel-update-tests pass, the pixel value is written to the framebuffer.

The output pixel value from the RE3 is written into a 5-way interleaved framebuffer, which stores a total of 56 bits (including the Z-buffer) for every pixel on a 1280 x 1024 viewing screen. The make-up of these 56 bitplanes is described below.

Image Planes

There are 24 bitplanes for storing the color information for every pixel. In a single-buffered RGB mode, these planes store a full-color 24-bit image. In a double-buffered RGB mode, the front and back buffer are each allotted 12-bits. Incoming 24-bit pixel values are dithered into 4-bit red, 4-bit green, 4-bit blue format producing nearly 24-bit resolution in each 12-bit buffer. For color index modes, the 24 bitplanes provide two full 12-bit color index buffers, one for the front buffer and one for the back buffer.

Depth Planes

A 24-bit signed Z-Buffer is a standard feature in the both XZ and Extreme Graphics. The 24-bit Z coordinate associated with each pixel is stored in the Z-Buffer planes. When hidden-surface removal is performed, the Z coordinate of an incoming pixel is compared to the current depth value already stored in the bitplanes. If the incoming Z coordinate is closer to the user's viewpoint, and therefore visible, the color value of the new pixel is used to update the image bitplanes, and the new Z coordinate value is written into the depth planes at the same location. Conversely, if the incoming Z coordinate is farther from the viewer, the new color value is ignored.

When running non-Z-Buffered applications, these 24 depth planes may be used as a second full-color 24-bit set of color planes, used identically to the standard color framebuffer.

Note: As stencil planes are added through IRIS Graphics Library control, they are stolen from the low order bits of the Z-buffer, with an effect on Z-buffer resolution.

Stencil Planes

XZ and Extreme Graphics support from 1 to 4 stencil planes. These planes reside in the low-order bits of the Z-Buffer. The Raster Engine has the ability to conditionally clear, write, increment, or decrement these planes independent of Z depth value. This capability allows pixels to be tagged as a way of extending the capability of the depth buffer to do a number of prioritizing algorithms.

Overlay/Underlay Planes

The framebuffer dedicates four bits per pixel to overlay or underlay operations. These planes are provided for use by a window manager or by applications that use features such as pop-up menus.

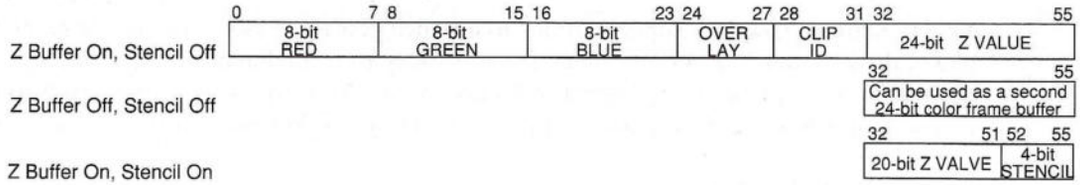
Window Clipping Planes

Four-bit planes hold data that define the boundaries of the windows on the screen. Each window opened is assigned a 4-bit clipping ID (CID). Every pixel associated with that window not covered by another window has its CID value written into the window clipping planes. For incoming pixels, the stored CID value is compared to the CID value of the incoming pixel. If a match occurs, the incoming pixel is written to the framebuffer; otherwise, the framebuffer is left unchanged. The window clipping planes are used in conjunction with the two screen masks to provide a very general window clipping mechanism.

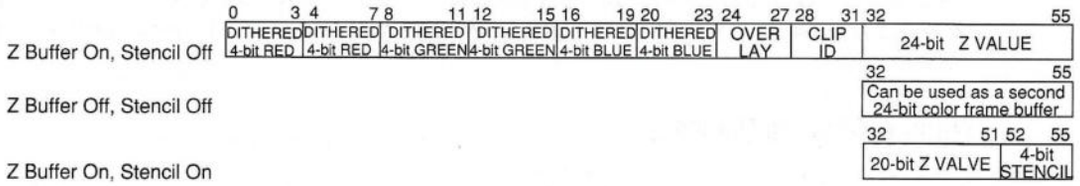
Framebuffer Configurations

There are 56 bits stored for each pixel location . The allocation of these 56 bits is shown below for various different modes.

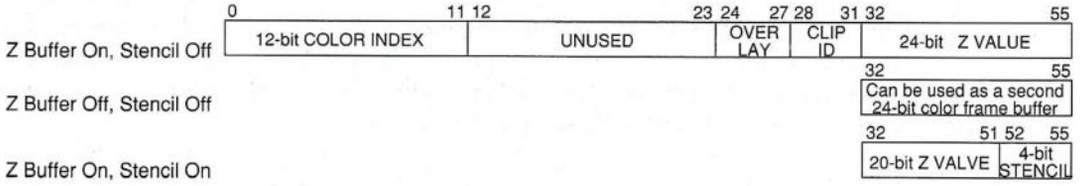
SINGLE BUFFERED RGB


Z Buffer On, Stencil Off
0 7 8 15 16 23 24 27 28 31 32 55
8-bit RED
8-bit GREEN
8-bit BLUE
OVER LAY
CLIP ID
24-bit Z VALUE
Z Buffer Off, Stencil Off
32 55
Can be used as a second 24-bit color frame buffer
Z Buffer On, Stencil On
32 51 52 55
20-bit Z VALVE
4-bit STENCIL

DOUBLE BUFFERED RGB


Z Buffer On, Stencil Off
0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31 32 55
DITHERED 4-bit RED
DITHERED 4-bit RED
DITHERED 4-bit GREEN
DITHERED 4-bit GREEN
DITHERED 4-bit BLUE
DITHERED 4-bit BLUE
OVER LAY
CLIP ID
24-bit Z VALUE
Z Buffer Off, Stencil Off
32 55
Can be used as a second 24-bit color frame buffer
Z Buffer On, Stencil On
32 51 52 55
20-bit Z VALVE
4-bit STENCIL

SINGLE BUFFERED COLOR INDEX


Z Buffer On, Stencil Off
0 11 12 23 24 27 28 31 32 55
12-bit COLOR INDEX
UNUSED
OVER LAY
CLIP ID
24-bit Z VALUE
Z Buffer Off, Stencil Off
32 55
Can be used as a second 24-bit color frame buffer
Z Buffer On, Stencil On
32 51 52 55
20-bit Z VALVE
4-bit STENCIL

DOUBLE BUFFERED COLOR INDEX

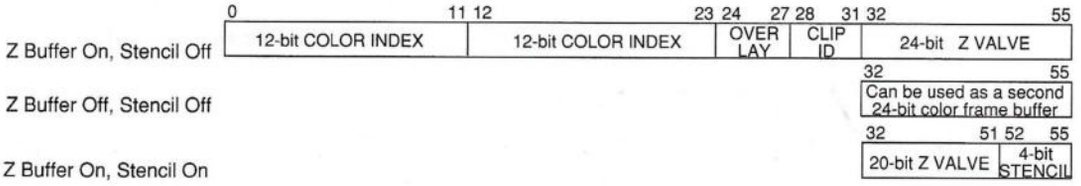

Z Buffer On, Stencil Off
0 11 12 23 24 27 28 31 32 55
12-bit COLOR INDEX
12-bit COLOR INDEX
OVER LAY
CLIP ID
24-bit Z VALVE
Z Buffer Off, Stencil Off
32 55
Can be used as a second 24-bit color frame buffer
Z Buffer On, Stencil On
32 51 52 55
20-bit Z VALVE
4-bit STENCIL

FIGURE 14 Framebuffer configurations.

5.6.4 Display Subsystem

The Display Subsystem receives pixel information from the framebuffer, routes it through the appropriate display mode, and sends it to Digital-to-Analog converters for display.

Video Timing Control

Video timing control, window display mode control, and cursor control are handled by the VCI gate array. Video timing determines the relationship between active pixels, blanking periods, and sync times. These relationships vary from monitor to monitor.XZ and Extreme Graphics provide support for the following monitor types:

- 72 Hz 1280 x 1024
- 60 Hz 1280 x 1024
- 72 Hz 1024 x 768
- 60 Hz 1024 x 768
- NTSC (unencoded)
- PAL (unencoded)
- 120 Hz 1280 x 1024 stereo
- 120 Hz 1024 x 768 stereo

The VCI stores a window display mode for every pixel on the screen in a run-length encoded table. This display ID (DID) value determines the color mode format used to interpret the data from the image bitplanes. The DID value is passed to the Multimode Graphics Processors that interpret the image bitplanes based on the DID value. X–Class and E–Class Graphics display multiple images simultaneously, in an overlapping window environment, in single-buffered RGB, double buffered RGB, single-buffered color index, and double-buffered color-index color modes. Simultaneous display of up to 32 unique window styles is allowed.

The VCI controls a cursor memory capable of storing a 32 x 32 three-color cursor glyph. Cursor data is fed into the pixel stream through Multimode Graphics Processors.

Multimode Graphics Processor

Five Multimode Graphics Processors (XMAP7) concurrently receive cursor information from the VCI. The DID values determine how the image data is routed and presented to the Digital-to-Analog Converters. If the overlay/underlay planes are active, they take precedence over the image planes. A 16 x 24 auxiliary lookup table is included for determining overlay/underlay color. The cursor takes the highest precedence and supplants both the image and overlay/underlay planes. The MGPs hold 3 x 24 lookup table for cursor color.

Digital-to-Analog Converters

High-speed Digital-to-Analog Converters (DACs) drive the red, green, and blue electron guns of the color display. When the Graphics Subsystem operates in RGB color mode, the DACs receive up to 24 bits of color information for each pixel. Eight of these bits are directly assigned to each of the red, green, and blue DACs to yield more than 16 million colors. The DACs are multiplexed to handle the input from the five parallel pixel pipes. In color-index mode, pixel data packets are used as indices into a 12-bit-in, 24-bit-out color map before being sent to the DACs. This map defines 4096 simultaneously visible colors from a palette of 16.7 million. The pixel-mapping feature of the color-index mode allows screen colors to be quickly modified by simply changing the values stored in the color maps.

The XZ and Extreme Graphics subsystems uses RAMDAC technology to provide gamma correction under application control. Any 8-bit-to-8-bit mapping can be specified and is applied both to RGB and color index pixels.

Live Video I/O Slot

The XZ and Extreme Graphics design provides a port for RGB pixels to be extracted from the Video Bus data stream. This capability allows a Live Video I/O board to be plugged into the Video Bus for real-time capture of the contents of the graphics framebuffer (which can then be sent to the video card), and real-time display of video input on the main graphics monitor.

Genlock

Genlock is available for low resolution video signals; Vertical Frame is available for high resolution video signals.

Stereo Viewer

Indigo^2 is shipped stereo-ready with a multi-sync high-resolution monitor. To actually utilize the stereoscopic viewing option, users must obtain the StereoView option, including an LED emitter synchronized to the monitor refresh rate of 120Hz and a pair of lightweight LCD shutter glasses.

5.7 XZ and Extreme Graphics Features

5.7.1 MicroPixel Sub-Pixel Positioning

After being projected to the screen by the Geometry Subsystem, all vertices retain their fractional positioning information instead of being coerced into integers. This gives an accurate description of the primitive's position in a floating-point space. Without this feature, primitives would be rendered incorrectly and would jitter as they move, also causing serious problems with the anti-aliasing features described below.

5.7.2 Blending

The pixel data in the framebuffer is replaced with weighted average of itself and the pixel data being drawn. The user selects the function controlling both the source and destination factors used in the blend.

One common blend operation uses the alpha component of the pixel being drawn as the source factor and one minus alpha as the destination factor. The greater the alpha value, the more weight is given to the incoming data in the blend. This method is used to draw anti-aliased lines and to generate transparencies. It can be used anytime subpixel coverage is demanded.

Blending results are best when drawn into a 24-bit framebuffer, especially when blending in multiple passes. For this reason, it is best to perform the blending in single-buffer RGB mode. For those who require smooth motion and are not drawing with Z-buffering enabled, it is possible to blend the pixel data into the Z-buffer and copy each completed frame from the Z-buffer to the framebuffer. Because of the fast pixel copy rates, this method achieves smooth motion.

5.7.3 Point Anti-Aliasing

To render an anti-aliased point, a 2 x 2 grid of pixels is used to approximate the area covered by a filtered point. The four pixels are given blend weights proportional to the distance from their pixel centers to the actual point location in sub-pixel space.

5.7.4 Line Anti-Aliasing

Lines are anti-aliased by drawing a multi-pixel-wide line with higher weights for pixels closer to the line in the minor axis, and lower values toward the outer pixels. Effectively, we are approximating the location of a line by a wide line that is filtered in the minor axis. Similar to points, RGB lines are blended into the framebuffer by the weights. For color indexed anti-aliased lines, instead of generating a weight for blending, the hardware substitutes the lower 4 bits of the color index value. The new color then indexes into a ramp in the color look-up tables.

Slope Correction

As the slope of a line gets closer to 45 degrees, pixels that approximate the line should get brighter since fewer pixels span the same length on a raster screen. To achieve this, the coverage terms are adjusted by the slope of the line. The weights are higher for diagonal lines and lower for horizontal and vertical lines. A hardware lookup table uses the line slope to correctly generate the weights, and later blend them into the framebuffer. For color indexed lines, the slope is also a factor in determining the new color index value.

Endpoint Filtering

So far, the weights of pixels that make up anti-aliased lines have been adjusted only in the minor axis. The endpoints of the lines must also be adjusted in the major axis to avoid popping from one pixel to the next. To correct this, the hardware uses the subpixel information in the major axis to adjust the intensity of the endpoint color. This way the apparent endpoint moves gradually from one pixel to the next.

5.7.5 SharpScene Accumulation Buffer

XZ and Extreme Graphics use the CPU main memory as an accumulation buffer to combine or accumulate a set of scenes. The IRIS Graphics Library API also allows for a weighted blend of each of the scenes into the accumulated image. The weight of each scene is defined by the user. These weights can be used with other features of the graphics subsystem (i.e., projection matrix) to define User-Programmed Filter Functions.

When using the accumulation buffer in a double-buffered mode, 12-bit RGB images in the graphics framebuffer are accumulated into 32-bit RGB images in CPU main memory, resulting in a certain loss of image quality. Single-buffered applications make use of the full 24-bit color.

Progressive Refinement

As each frame is accumulated into the SharpScene buffer, a more accurately sampled image is produced. The user can choose to render fewer frames to support real-time constraints, or to render many frames to obtain a high-quality image.

Multi-Pass Spatial Anti-Aliasing

Multi-Pass Spatial Anti-Aliasing is done by rendering the same objects for several frames while moving them spatially. By jittering the subpixel offsets (i.e., projection matrix) and accumulating the scenes together, an anti-aliased image is rendered. Furthermore, the user can choose a desired filter function to define the weights for each pass.

Optical Effects

By modifying the projection matrix as images are accumulated, viewing the scene from various points across the aperture of a lens, the sense of depth of field is created. Objects that are further from the focal plane of the lens are blurred while closer objects are made sharper.

Convolutions

An image can be quickly filtered using the accumulation buffer. Since the user has control of the weighted accumulation of each image, and the image can be moved about on screen in multiples of pixel coordinates, the accumulation buffer can be used to convolve the image using many filtering techniques.

Orthogonality

The accumulation buffer provides a solution for the problem of spatial aliasing, motion-blur, depth of field, and penumbra. Another feature of the accumulation buffer is that all these techniques can be used together in any combination to render a high-quality image.

5.7.6 Lighting Features

The XZ and Extreme Graphics architecture supports a wide range of lighting capabilities to enable the realistic rendering of geometric primitives. Lighting effects are computed on a per-vertex basis (Phong lighting) and are thus supported in the Geometry Engines.

XZ and Extreme Graphics support all of the following IRIS Graphics Library API lighting capabilities in hardware.

Light Sources

Up to eight light sources may be used simultaneously. The user can specify the color and position of each light source.

Surface Properties

The IRIS Graphics Library API allows the user to configure a number of surface properties to achieve a high degree of realism. Specifically, the user can define the emissivity of a surface and its ambient, diffuse, or specular reflectivity, as well as its transparency coefficients. A shininess coefficient is provided to specify how reflective an object is. The Command Processor and Geometry Engines were specifically designed so that surface properties can be modified on a per-vertex basis very quickly. This feature is particularly useful for scientific visualization. For example, an aeronautical engineer can change the diffuse reflectance at every vertex to show the stress contour across an airplane wing.

Two-Sided Lighting

The user can specify different surface properties for the front and back sides of geometric primitives to display objects whose inside and outside colors differ. This obviates the need to specify and render two separate primitives.

Local Light and Viewer Positioning

Traditionally, hardware-supported lighting models assume that the viewer and light sources are positioned infinitely far from the object being illuminated. Although the positioning of the viewer and/or light sources at a finite distance from the object can enhance the realism of the scene, these models are often avoided because of costly inverse square root operations. The XZ and Extreme Graphics Geometry Engines include special VLSI support for computing inverse square roots, thus speeding local lighting calculations enormously.

5.7.7 Atmospheric Effects

The IRIS Graphics Library API simulates those fog and haze effects required for visual simulation applications by blending the object color with a user-specified fog color. The user also enjoys control over the fog density through the IRIS Graphics Library interface.

5.7.8 Texture Mapping

Motivation

The entire Indigo product line offers a software implementation of texture mapping that is capable of generating images of the same high quality as those produced on Silicon Graphics' high-end visualization products. Texture mapping has traditionally been used in fields such as visual simulation and computer animation to enhance scene realism. Textures can add vegetation and trees to barren terrain models without adding geometric complexity. Labels can be applied to computer-modeled package designs to get a better appreciation of how products will actually look. Patterns mapped onto geometric surfaces can provide additional motion and spatial cues that surface shading alone can't offer. For example, a sphere rotating about its axis appears static when displayed as a shaded surface; however, by affixing a pattern to the sphere, its motion can be easily detected.

Quality

It is essential that errors be minimized during the texture-mapping process. Perspective correction of texture coordinates is performed during the scan-conversion process to prevent textures from "swimming" as an object moves in perspective.

Texture aliasing is minimized by filtering the texture for each pixel textured. Without filtering, textures on surfaces appear to sparkle as surfaces move. Filtering is accomplished using a mip-mapping technique. Prefiltered representations of a texture are computed at different levels of resolution. For each pixel textured, an interpolated texture value is derived by sampling pixels from the two maps closest to the required texture resolution. Textures can have 8, 16, 24, or 32 bits per pixel.

Flexibility

A variety of texture types and environments are provided to support the diverse applications of textures. Textures can be defined to repeat across a surface or to clamp outside of a texture's unit range. Textures can be in monochrome or color, with alpha or without. Texture alpha can be used to make a polygon's opacity vary at each pixel. For instance, when an RGBA image of a tree is mapped onto a quadrilateral, objects behind the polygon can appear through the polygon wherever the opacity of the tree map is low, thereby creating the illusion of an actual tree.

Textures can be combined with their surfaces in a variety of ways. A monochrome texture can be used to blend between the surface color and a constant color to create effects such as grass on dirt or realistic asphalt. By adding alpha, a texture can be used to create translucent clouds. Textures can also be used to modulate a surface's color or be applied as a decal onto a surface.

The XZ and Extreme Graphics architecture can automatically generate texture coordinates, based on user-specified behavior. This feature can be used to texture map contours onto an object without requiring the user to compute or store texture coordinates for the object.

5.7.9 Stencil Planes

The stencil bitplanes implemented in the Raster Subsystem depth buffer allow a new mechanism for affecting the results of pixel algorithms. In many ways, the stencil can be thought of as an independent, high-priority Z-buffer. The stencil value can be tested during each pixel write, and the result of the test determines both the resulting stencil value, and whether the pixel algorithm will produce any other result.

One application of the stencil is Z-Buffered image copy. With one pass, the stencil planes record the result of depth comparisons between source and destination areas of the framebuffer; with a second pass, the image is copied from source to destination, with only the pixels that passed the depth comparison being updated. As an example, this method can be employed with a library of small 3D images, such as spheres and rods, to quickly construct molecular models in the framebuffer.

A second application is the ability to draw hollow polygons—useful for visualizing the structure of solid models. By drawing the outline of each facet into the stencil, and subsequently performing Z-Buffered drawings of the whole facet while using the stencil as a mask, the true joining edges of an object's surface can be displayed alone, highlighted, or with the background color filled to expose a hidden-line representation.

Most significantly, the stencil mechanism allows Constructive Solid Geometry pixel algorithms to be implemented in a parallelized environment. The flexible testing and updating constructs designed into the Image Engines allows the construction of unions and intersections of primitive shapes, all with the attributes of texture mapping, transparency, and anti-aliasing.

5.7.10 Arbitrary Clipping Planes

The Geometry Subsystem supports the definition of six planes in 3D space. Geometric primitives can be clipped against these planes in addition to the normal six planes that describe the current viewing volume, providing an ideal mechanism for viewing the cross-section of model components or volumetric data.

Alternatively, the distance between a primitive and any plane can be calculated. This distance can be used as a texture-mapping coordinate, which then can be used to produce a contour map applicable to any 3D model for improved visualization.

5.7.11 Pixel Read, Write, and Copy

XZ and Extreme Graphics offer a host of features that greatly enhance the pixel read, write, and copy operation. At the core of these features is a 32-bit DMA channel that provides ultra high-speed pixel transfers between the host, the framebuffer, and the Z-buffer. In addition to the standard 32-bit pixel, packed pixels of sizes 16, 8, and 1-bit are supported. During the transfer, 1-bit pixels can be expanded into one of two 32-bit packed RGBA values defined by the user. Future IRIS Graphics Library releases will support 8-bit to 32-bit expansion (pixel look-up) during transfer.

Those interested in large data sets will discover that pan and zoom are supported by the hardware at interactive rates.

For pixel reads or writes, the screen-relative direction of the read or fill (right-to-left or left-to-right, bottom-to-top or top-to-bottom) is user selectable. Copies from the Z-buffer to the framebuffer are oriented from left-to-write and top-to-bottom. If Z-Buffering is not required, the user can draw a 24-bit image into the Z-buffer, then copy it to the framebuffer one frame at a time. By synchronizing the copy to the screen refresh, it is possible to achieve the effect of true 24-bit double-buffering. This is especially useful when doing multiple-pass blending operations.

Sphere Rendering

XZ and Extreme Graphics support high-speed rendering of high-quality spheres. Its intelligent frame buffer allows a sphere to be rendered as a "2 1/2 D" image, i.e. a two-dimensional array of pixel data with a depth value associated with each pixel. These images are rendered using the standard z-buffer algorithm.

Section 6 Software Environment

Indigo^2 offers exciting software solutions to complement the powerful Indigo^2 hardware and enhance the working and development environment.

The full hardware power of Indigo^2 is made available through bundled end-user tools such as IRIS Showcase™ 3.0 and IRIS Media Mosaic. Several products for the developer are available, including CASEVision tools, programming and media libraries.

The extensive set of software available with the Indigo^2 workstation allows both developers and end-users to add interactive 3D, high-resolution images, audio, and video to applications and presentations.

Industry standards are utilized throughout Indigo^2 software. From Unix to X11 to standard image and audio file formats, Indigo^2 provides a standards based environment that allows for easier integration into a heterogenous work environment as well as easier development and maintenance of applications.

As a member of the IRIS 4D workstation family, Indigo^2 is binary-compatible with other IRIS 4D workstations; applications written for existing IRIS workstations run with little or no modification on Indigo^2, and applications written on an Indigo^2 also run on other IRIS 4D systems. Because an Indigo^2 supports most of the advanced graphics features found on IRIS Advanced Graphics™ systems, you can use the less expensive Indigo^2 to run advanced graphics applications or to develop applications for more expensive IRIS 4D systems.

Indigo^2 workstations come with a rich set of system and application software installed on disk. They present end-users with an intuitive and visually pleasing graphical interface to the operating system, which makes desktop file operations and system configuration fast and simple. The development option offers programmers an extensive set of both industry-standard and proprietary libraries as well as development tools to quickly construct applications of any size and complexity.

6.1 End User Tools

6.1.1 IRIS InSight™ Viewer

Now you can access Silicon Graphics end user manuals, customer support, and product information directly on your workstation using IRIS InSight Viewer. Remarkably easy to use, IRIS InSight Viewer offers fast access to online documents. IRIS InSight Viewer and Document Library are shipped with all new graphics systems. You can choose to access your online manuals from your system disk, a server, or directly from CD-ROM.

6.1.2 Space Tour

SpaceTour is an interactive tour of the Indigo^2 workstation. It familiarizes users with Indigo^2 through system set-up and configuration demonstrations. SpaceTour also introduces users to free Silicon Graphics software as well as 3rd party products. Information about available Silicon Graphics' services is also included.

6.1.3 WorkSpace

IRIS WorkSpace provides an icon-based graphical interface to the IRIX file system. Users can traverse directory trees, find, copy, and move files, and launch applications with a click of the mouse. IRIX 5.1 includes an enhanced version of WorkSpace, including features such as arbitrary zoom on file structures, and IconSmith, a graphical icon editor.

6.1.4 System Manager

IRIS System Manager simplifies system administration tasks that can be cumbersome on a standard UNIX system. By clicking on icons and filling in text fields, users can perform such tasks as file system backup, network monitoring and administration, and user account management. Both WorkSpace and the System Manager can be used remotely from any IRIS workstation on the host workstation's network.

6.1.5 IRIS Showcase™ 3.0

IRIS Showcase™ 3.0 allows you to create interactive documents that incorporate text, raster images, digital audio, live video graphics, and 3D objects. A Showcase document can be viewed as an interactive presentation or an onscreen slide show, captured on video tape for a video presentation, printed as a paper document or overhead, or encoded as ASCII and sent as an email message.

Showcase 3.0 allows you to create, import, and edit Inventor-based 3D models. You can use your primary application to develop model data and then import the data into Showcase to take advantage of Showcase's editing and interactive presentation features. Showcase 3.0 3D editing capabilities include: a material editor, a material palette, a texture editor, and palette, an extrusion profile editor, and a light and shadow editor. Translators to the Inventor file format for DXF, IGES, and several applications are available.

Showcase HyperScripts allow you to create interactive documents that include scripted actions linked to objects on a page. HyperScript actions include page turns, launching other applications, playing video, playing audio and many others.

Showcase also supports a wide selection of font families and point sizes. Fonts can be rotated, scaled interactively, and converted to 2D graphics.

6.1.6 IRIS Media Mosaic

IRIS MediaMosaic is a set of powerful easy-to-use tools which provide basic production capabilities for a range of media. This product set allows for a plug and play, with NTSC or PAL video input and output. Users can also grab video frames, create and edit movies, and create audio annotation. The Video Control Panel, Video Pro Panel, Movie Maker, Movie player, Audio Control Panel, SoundEditor and SoundFiler, CD Manager and DAT Manager are included.

6.1.7 ImageTools

IRIS Image Tools make it easy to capture, create and manipulate standard-format images, supporting image scan, blur, rotate, scale, stretch, sharpen, and more.

6.1.8 Digital Media Clip Library

With over 20 MB of ready-to-use images, sounds, movies and 3D objects, the Digital Media Clip Library takes you several steps closer to compelling interactive presentations.

6.1.9 IRIS Explorer

IRIS Explorer™ is a modular application builder that enables end users and developers to rapidly prototype applications and reconfigure their software environment. Explorer greatly simplifies using Silicon Graphics systems to create new applications, visualize changing data sets, integrate foreign data types, and much more. Users can:

- Build applications from a series of reconfigurable modules
- Visualize data sets in new and unique ways
- Publish modules for use by others
- Obtain tangible results in minutes—without programming
- Work in a distributed execution environment
- Use existing code as a basis for new modules

The IRIS Explorer environment is a new paradigm for using computers. Modules supporting Computational Fluid Dynamics, Molecular Modeling, EOS-DIS Earth Sciences, Medical Imaging, and more can be combined with user-created modules to build applications and to explore science in ways that change as fast as the users' needs.

6.2 Developer Tools

Indigo^2 offers a productive software environment for many kinds of software development. For UNIX programming, it provides IRIX 5.1, Silicon Graphics' version of SVR3 UNIX with 4.3 BSD extensions, and other extensions that include TCP/IP network protocols and Network File System™ (NFS™). For window management, it provides a full implementation of the X11/R5 Window System, Display PostScript™, and 4Dwm™, a Motif™-based window manager. To resolve any potential color conflicts between X11 and 3D graphics applications, Indigo^2 keeps completely separate color maps for both X11 and IRIS Graphics Library™ applications.

For graphics programming with the XL Graphics configuration, Indigo^2 offers a software-based implementation of the IRIS Graphics Library (GL™). It offers support for input devices such as the mouse, keyboard, spaceball, trackball, and digitizing tablet. It also provides calls for object modeling in 3D space for spatial transformations (providing perspective and viewpoint control, etc.), for lighting, rendering polygonal and spline surfaces, smooth animation, and many other graphics tasks. It provides the full set of IRIS Advanced Graphics graphics features (with the exception of stencil-plane and alpha source-blending functions), which include fogging and multiple arbitrary clipping planes. In addition, with IRIX 5.1, IRIS GL graphics can be displayed within subwindows of X applications, allowing IRIS GL programmers to take advantage of Motif and other X11-based user interface toolkits, and X programmers to make use of high-performance graphics.

For image processing on an Indigo^2, the SGI ImageVision Library™ offers an object-oriented extensible toolkit for creating, processing, and displaying images. Its core set of over 70 routines provides general-purpose image operators which are easily augmented using abstract data types (objects) and access functions (methods). It also provides a general interface for image-processing applications, support for SGI, TIFF, and FIT formats, an optimal memory model for handling large images, and an architecture that supports general image types.

6.2.1 CASEVision

Silicon Graphics' expertise in visual processing technology provides an advanced, interactive, visual development environment with CASEVision™. CASEVision brings the advantages of visualization to software developers by providing the ability to see processes and data structures.

Premiere third-party CASE products supplement Silicon Graphics' solutions. The ToolTalk integration mechanism allows both Silicon Graphics' and third-party solutions to be tightly integrated so users can concentrate on the job at hand instead of managing the boundaries between the individual tools. The CASEVision environment is optional and composed of the following major components:

CASEVision/Workshop is an Interactive programming environment that consists of a Static Analyzer, a visual Debugger, a Performance Analyzer and a Build Analyzer.

CASEVision/ClearCase is an advanced Configuration Management, Version Control and Build Management system designed to support large-scale development.

CASEVision/Tracker is a flexible event tracking system that is tightly integrated with other CASEVision solutions.

6.2.2 Compilers and Standard Development Tools

Silicon Graphics supplies a variety of compilers to best suit your programming needs. ANSI standard C and Fortran compilers are available, as well as compilers for C++, Ada, and Pascal.

IRIX 5.1 includes a set of profiling tools that can identify CPU-intensive code fragments to help focus optimization efforts. Prof and pixie provide detailed analyses of application performance. Grosview gives a view of system loading; users can see what percentages of the available CPU, I/O, and other resources are being used at any given time.

IRIX 5.1 also includes general and specialized debuggers. Dbx, a standard UNIX source-level debugger is included. In addition, IRIX 5.1 comes with gldebug, specifically designed for debugging graphics applications created using the IRIS Graphics Library. It includes a viewer which graphically displays the state of the IRIS GL as the application is running, and a controller, which lets you interactively set break points and change the level of debugging output.

6.2.3 The Iris Graphics Library

The IRIS Graphics Library (GL) is a set of over 300 function calls available in C, C++, Fortran77, Ada, and Pascal versions. The IRIS GL simplifies the development of highly interactive real-time graphics applications. It supports input devices such as the mouse and keyboard, digitizing tablets, dial and button boxes, and the spaceball. When used in conjunction with a toolkit like IRIX/Motif, the IRIS GL lets developers create highly responsive graphics applications with industry-standard user interfaces.

IRIS GL programmers define object, world, and viewing coordinate systems, and apply orthographic or perspective projections to map them to any viewport on the screen. Objects can be translated, rotated, and scaled in real time, without flicker, by taking advantage of high-speed IRIS GL 3D rendering capabilities and double buffering. IRIS GL includes powerful primitives that allow programmers to create points, lines, arcs, circles, polygons, parametric curves, rational bi-cubic patches, and Gouraud shaded, Z-buffered solids. Complex objects can be quickly built by combining these primitives.

Advanced Graphics Features

Indigo^2 supports most IRIS GL functions, including IRIS Advanced Graphics functions found on high-end IRIS workstations. All Indigo^2 workstation configurations support the following Advanced Graphics features:

- Lighting models
- Texture-mapping
- Accumulation buffer
- Alpha blending
- Fogging
- Arbitrary clipping planes
- Anti-aliased lines
- Depth cueing
- Subpixel positioning
- Stenciling
- Source alpha blending
- Anti-aliased points
- Pixel read, write, and copy

Network Transparency

In IRIX 5.1, the IRIS GL is network-transparent; any IRIS GL program may be run remotely from another IRIS 4D workstation sharing the same network as the host workstation. Users can set the DISPLAY variable in their environment to the name of the workstation to which they want to send IRIS GL (and X11) applications to be imaged (the IRIS GL works remotely only on other IRIS workstations running IRIX 5.1).

6.2.4 Open GL

Open GL is an application programming interface (API) providing 2D and 3D graphics functions to software programmers. Functions include modeling, transformations, color, shading, lighting, texture mapping, and sophisticated framebuffer operations such as alpha blending and motion blur. All functionality is supported across the IRIS workstation family, as well as all other Open GL implementations on other workstations and personal computers.

6.2.5 IRIS Inventor

IRIS Inventor is an object-oriented software library that drastically simplifies graphics programming. It is the catalyst for writing highly interactive, creative graphics applications. This programming environment provides a rich set of pre-programmed building blocks, and defines a full featured, extensible framework through which entire applications can be developed.

6.2.6 Image Processing Library

The ImageVision Library™ object-oriented extensible toolkit is for creating, processing, and displaying images on all IRIS 4D workstations. The toolkit provides a framework for managing and manipulating images to aid image processing applications developers. Some of the features it provides are:

- A common functional interface for image processing applications across the IRIS 4D product line.
- A core set of general purpose image operators and an easy way to add new operators. The first release contains a core set of about 70 routines. A set of abstract data types (objects) and access functions (methods) are provided to allow a developer to design and augment the set of image operators.
- Support for three standard image formats: SGI, TIFF, and a tiled format based on TIFF called FIT. New file formats can be seamlessly integrated into the library as needed.
- An optimal memory model for handling large images. ImageVision Library provides a memory model for efficient manipulation of general image data types, sizes, and resolutions. It includes a configurable cache to allow access to and processing of very large images.
- An architecture that supports general image types. ImageVision Library provides an interface for manipulating image attributes and image data requiring little or no knowledge of the internal structure and format of the image.

6.2.7 Digital Media Libraries

Several libraries are available for Indigo^2 workstations to assist programmers in developing multimedia applications incorporating 2D and 3D graphics and audio, as well as support for video I/O devices. Key among these are the Audio Library, the IndigoVideo Library, the MIDI Library and Compression Library, and the Image Processing Library.

The Digital Media Development Option offers a comprehensive and intelligent environment for digital media application development on the Indigo^2 Workstation. Six library modules callable from C and C++ enable the rapid development of audio, video and MIDI applications that need to use the Indigo^2 workstation's unique hardware features. DMDEV gives you the power to access the world of digital media.

The Audio Library and Audio File Library access the basic capabilities: reading and writing samples from the hardware and reading and writing disk files in AIFF and AIFF-C formats. The CD-ROM Audio Library and DAT Audio Library provide transport control and access the audio capabilities of the optional CD-ROM and DAT drives. The MIDI Library supports reading and writing of time-stamped MIDI messages through Indigo^2 serial ports using a Macintosh® serial port to MIDI converter. it also assists with the parsing of incoming MIDI messages.

6.3 Operating System

6.3.1 IRIX 5.1

IRIX is Silicon Graphics' implementation of the UNIX operating system, first developed by AT&T Bell Laboratories. IRIX 5.1 is based on AT&T UNIX System V.4, but also includes numerous 4.3 BSD extensions, such as TCP/IP network protocols and Network File System (NFS), which provide transparent access to files across a heterogeneous network. Adherence to these industry standards lets users easily integrate an Indigo^2 into existing computing environments.

In addition to the BSD extensions, IRIX includes several enhancements to support the real-time requirements of 3D graphics and audio:

- Non-degrading priorities and high-resolution timers
- Kernel primitives and libraries that support multi-process applications and high-performance concurrent programming
- Memory-mapped files that allow a process to access a file as part of its address space
- A tight coupling between the operating system and IRIS Graphics Library kernel routines to produce high graphics throughput

IRIX applications are binary compatible across the entire IRIS 4D product line, making it trivial to move existing applications to an Indigo^2 and to port applications developed on an Indigo^2 to more expensive machines.

The Indigo^2 operating system, IRIX 5.1, is a standards-rich user and programming environment, compliant with the following window system and operating system standards:

- X11/R5
- IRIX/Motif, based on OSF/Motif Release 1.2.2
- Display PostScript
- AT&T UNIX System V.4, with 4.3 BSD enhancements
- POSIX 1003.1
- X/OPEN XPG3, Vol. 1,2,3

6.3.2 The X Window System

With the release of IRIX 5.1, the X Window System™ runs native on all IRIS workstations. Indigo^2 was designed to run X11/R5 quickly and efficiently, and offers better X performance than other IRIS workstations. X11 support on an Indigo^2 and the rest of the IRIS family includes Display PostScript, the OSF/Motif user interface toolkit, and special extensions for supporting 3D graphics subwindows within X applications. Other extensions to X11 include arbitrary shaped windows, and input mechanisms for IRIS input devices such as tablets, dial-and-button boxes, and the spaceball.

4Dwm is an OSF/Motif-compliant window manager similar to the widely-used mwm, but offering enhanced usability and functionality for the end-user. 4Dwm, like most X-based window managers, is customizable to suit the individual user's taste.

IRIX/Motif

The IRIX/Motif toolkit offers an industry-standard API for constructing graphical interfaces. The Motif library is included as part of the Graphics Development Option for Indigo^2 and other IRIS 4D workstations. Interactive user-interface builders are also available as an option.

Display PostScript

The Display PostScript (DPS) server from Adobe is shipped as part of the IRIX 5.1 window system. Silicon Graphics is the first company to offer full 24-bit color support in Display PostScript under X. The DPS library is included as part of the Graphics Development Option for Indigo^2, and can be used in conjunction with X and Motif to create complete 2D applications.

X11 and the IRIS GL

IRIX 5.1 supports IRIS GL imaging and X-based graphics in separate subwindows of the same parent X window. To make this possible, Silicon Graphics provides a IRIS GL widget and several function calls for easy integration into X applications. This allows applications to use IRIX/Motif for a common, portable, and interoperable user interface and the IRIS Graphics Library for high-performance 3D rendering.

X11 and the Open GL

The Silicon Graphics implementation of X11/R5 fully supports GLX, the Open GL extension to the X Window System.

6.4 Networking

IRIX 5.1 provides TCP/IP and a complete suite of Internet and BSD network application programs. For administering medium to large networks, Silicon Graphics' offers NetVisualyzer™, which allows the user to interactively locate and correct network bottlenecks and breakdowns, and to analyze network usage via graphical displays of the entire network.

Indigo^2 workstations connect out of the box to Ethernet networks. In addition, several optional networking products are currently available:

- NFS™ with the Network Information System (NIS)™ allows file sharing, directory services, and data format interpretation.
- TCP 3270 software allows Indigo^2 workstations to connect to an IBM mainframe via Ethernet.
- SNA 3270, 3770, and LU6.2 software allows Indigo^2 workstations to connect to an IBM mainframe through an SNA gateway.
- 4DDN software allows Indigo^2 workstations to connect to a DEC system using DECnet™ protocols.
- Macintosh connectivity (third party solution)
- SNMP agent
- Distributed IRIS GL
- NetVisualyzer™ (visual traffic monitor)

The networking capabilities of an Indigo^2 workstation can also be expanded with the addition of an optional FDDI port.

For more information please call:
U.S. 1(800) 800-7441
Europe (41) 22-798.75.25
North Pacific (81) 3-5420.71.10
South Pacific (61) 2-879.95.00
Latin America 1(415) 390.58.28
Canada 1(416) 625-4747

Corporate Office
2011 N. Shoreline Boulevard
Mountain View, CA 94043
(415) 960-1980

SiliconGraphics
Computer Systems

© 1993 Silicon Graphics, Inc. All rights reserved. Specifications are subject to change without notice.
Silicon Graphics, the Silicon Graphics logo, and IRIS, are registered trademarks of Silicon Graphics, Inc.

INDIGO2-TR (06/93)